Three-phase Grid Forming Inverter

GFM_inverter1

AVM
45MVA
34.5kV
Droop based GFM

Hossein Ashourian, Henry Gras, 4/11/2022 11:10 AM

1 Description

This document presents a generic EMTP model for a three-phase aggregated grid-forming inverter (GFM inverter). It can be used for stability, fault, harmonic, dynamic, and interconnection studies. The converter is a three-phase voltage source converter (VSC). Its control system is based on the dq vector voltage-current-control approach. Thus, it can naturally limit the current flowing into the converter during disturbances. The basic principle of vector control is to regulate the instantaneous voltage angle and amplitude independently through a cascade control loop [1].

The GFM inverter can be modeled either as:
- droop-based
- virtual synchronous machine (VSM)-based
- dispatchable virtual oscillator (dVOC)-based
- or a PLL-based GFM inverter.

A generic primary-control model of GFM inverter presented in [2], [3], [4]is used for modeling.

The converter model can be either Detailed (DM), in which case the IGBT are represented, or Average-Value (AVM), in which case ideal voltage sources follow the voltage reference calculated by the inner-control loops. The DC link of the converter can be connected to either a battery energy storage device or a constant DC voltage source.

A step-up transformer may be included between the converter and Point of Interconnection (POI).

The necessary protection functions are added to converter. The model is valid for load-flow, time-domain and frequency scan simulation types.

2 Converter Pins and Device Mask

The section describes the converter pins and device mask.

2.1 Converter pins

This device has 4 pins:

Table 1 Converter model Pins

Pin name	Port type	Description	Units
P (+)	Single-phase power	Positive pole of the DC link	
N	Single-phase power	Negative pole of the DC link	
refs	Control input bundle	Pref: Active power, Qref: reactive power Vacref: AC voltage See here how to use bundle.	pu
PCC	3-phase power	Point of Common Coupling	

2.2 Parameters

General tab
- **Number of aggregated inverters:** Number of parallel-connected inverters
- **Frequency:** Grid frequency in Hz
- **Inverter AC voltage:** Voltage on the AC side of the inverter in kVRMSLL
- **Inverter rated power:** Rated apparent power of a single inverter in MVA, kVA, or VA

- **DC voltage:** DC-link voltage in kV
- **DC capacitor:** DC-link capacitor in kJ/MVA
- **Choke resistance:** Choke resistance in pu
- **Choke inductance:** Choke inductance in pu
- **Filter reactive power:** Reactive power generated by each inverter harmonic filter in MVAR, kVAR, or VAR. See 3.4.1 for more information on the filter
- **Number of inverters in service:** Number of parallel-connected inverters in service
- **GFM control method:** Droop-based, VSM-based, dVOC-based GFM, or PLL-based GFM
- **Initial active power:** initial inverter active power reference in pu
- **Initial reactive power:** initial inverter reactive power reference in pu
- **Initial AC voltage:** initial inverter AC voltage reference in pu
- **Adjust initial reactive power input with LF results:** if this option is checked, initial reactive power will automatically adjust based on LF results.
- **Use this device as a Slack bus in LF:** The device participates to the load-flow solution as either a Slack or PV bus. If this option is checked, the device participates to the load-flow solution as a Slack bus.
- **Initialization (participate in the load-flow solution):** Type of initialization.

  If 'Initialization (participate in the load-flow solution)' is selected, a load-flow bus and an ideal voltage source are added at the point-of-connection of the converter. At the beginning of the simulation, the ideal voltage source remains connected to hold the load-flow conditions until the converter is initialized.

  The initialization time is 0.05s. After this time, the ideal voltage source is disconnected.
- **Use control reference variations ($\Delta refs$) for inputs:** If this option is checked, the signals of the *ref* input bundle are control reference variations in pu. At any time, the outer loop control references are the initial references defined above plus these variations.

  If this option is not selected, the signals of the *ref* bundle are the references used by the outer loops. In this case, it is the user responsibility to make sure the initial references in the bundle match the one in the mask, the latter being used for load-flow and initialization, to avoid initialization problems.

Inverter Transformer tab

The 'Nominal three-phase nameplate input' transformer model from the standard EMTP library is used.

In the converter transformer tab, the data must insert for the one converter transformer. The converter model is aggregated. Therefore, the converter transformer is aggregated according to number of aggregated converters, which is automatically done by a script. The total nominal power of one aggregated converter transformer is equal to one converter transformer nominal power multiplied by the number of aggregated converters.

- **Include step-up transformer:** If this option is checked, the converter transformer included and connected between the converter and the grid.
- **Connection Type:** YgYg, DYg, YgD, or DD
- **Nominal power:** Nominal power of a single transformer in MVA
- **Nominal frequency:** Nominal frequency of the transformer in Hz
- **Grid side voltage:** Nominal voltage transformer on the grid side in kVRMSLL
- **Converter side voltage:** Nominal voltage transformer on the converter side in kVRMSLL
- **Winding R:** Winding resistance in pu
- **Winding X:** Winding reactance in pu
- **Winding impedance on winding 1:** Winding impedance on winding 1, distribution ratio
- **Magnetization data:** Current -flux data in pu-pu or A-Wb
- **Magnetization resistance:** Magnetization resistance in pu or Ω

- o **Exclude magnetization branch model:** If this option is checked, the magnetization branch model is excluded.

Converter Control tab
- o **Converter model:** AVM, average value model or DM, detailed model
- o **PWM frequency:** PWM frequency in Hz

Measuring and monitoring unit
- o **Sampling rate:** Sampling rate frequency in Hz
- o **Cut-off frequency:** Cut-off frequency of measuring input filters in Hz, first-order low-pass filter
- o **PLL proportional KP_{ll}:** PLL PI controller, proportional gain in pu
- o **PLL integral KI_{pll}:** PLL PI controller, integral gain in pu

Primary control (droop, VSM ,dVOC, PLL-based controls) (see 3.5.1.2)
- o **Filter cut-of frequency w_c:** active and reactive power filter cut-off frequency in rad/s
- o **Frequency droop coefficient d_F:** frequency droop coefficient in s/rad
- o **Voltage droop coefficient d_v:** voltage droop coefficient in pu
- o **VSM inertia constant m_F:** inertia time constant s^2/rad
- o **VSM damping factor d_d:** damping coefficient s/rad
- o **dVOC synchronization gain k_1:** synchronization gain in pu
- o **dVOC voltage amplitude gain k_2:** voltage-amplitude control gain in pu
- o **State freeze threshold V_{dip}:** state freeze threshold in pu
- o **Minimum frequency deviation dw_{min}:** minimum frequency deviation in rad/s
- o **Maximum frequency deviation dw_{min}:** maximum frequency deviation in rad/s
- o **Maximum output active power P_{max}:** Maximum output active power in pu
- o **Minimum output active power P_{min}:** Minimum output active power in pu
- o **Maximum output reactive power Q_{max}:** Maximum output reactive power in pu
- o **Minimum output reactive power Q_{max}:** Minimum output reactive power in pu
- o **Overload mitigation controller KP_{lim}:** Overload mitigation controller, proportional gain in pu
- o **Overload mitigation controller KP_{lim}:** Overload mitigation controller, integral gain in pu/s
- o **Freezing PQ limiter reset delay T_{frz}:** Freezing PQ limiter after voltage recovery in s

Inner control (voltage , active power and current controls)
- o **Current priority:** active power priority (Ppriority) or reactive power priority (Qpriority)
- o **Current limit:** Converter current limit in pu
- o **Current control setting method:** Rise time or PI regulation gains. If the rise time method is selected PI regulator gains automatically calculated based on the rise time.
- o **Rise time:** Closed-loop current control rise-time in ms
- o **Current control proportional gain KP_i:** current PI controller, proportional gain in pu
- o **Current control integral gain KI_i:** current PI controller, integral gain in pu
- o **Voltage control proportional gain KP_v:** voltage PI controller, proportional gain in pu
- o **Voltage control integral gain KI_v:** voltage PI controller, integral gain in pu
- o **Active power control proportional gain KP_p:** active power PI controller, proportional gain in pu
- o **Active power control integral gain KI_p:** active power PI controller, integral gain in pu

Protection tab
- o **Enable voltage sag protection:** If this option is checked, the voltage sag protection is enabled.
- o **Pickup DVS voltage:** Threshold voltage value to activate the Deep-Voltage-Sag (DVS) protection in pu

- o **Reset DVS voltage:** Threshold voltage value to deactivate the Deep-Voltage-Sag protection in pu
- o **Enable chopper protection:** If this option is checked, the chopper protection is enabled.
- o **Pickup Vdc:** Chopper ON when Vdc is above this value in pu
- o **Reset Vdc:** Chopper OFF when Vdc below this value in pu
- o **Enable overcurrent protection:** If this option is checked, the overcurrent protection is enabled.
- o **Converter pickup current:** Converter overcurrent protection threshold in pu
- o **Reset delay:** Overcurrent protection release delay in s
- o **Enable AC undervoltage protection:** If this option is checked, the AC undervoltage protection is enabled.
- o **AC undervoltage protection data:** Voltage versus time curve for the AC under voltage protection in s and pu
- o **Enable AC overvoltage protection:** If this option is checked, the AC overvoltage protection is enabled
- o **AC overvoltage protection data:** Voltage versus time curve for the AC under voltage protection in s and pu

Harmonics tab
- o **Use harmonic model for steady-state and time-domain simulations:** If this option is checked, this device is modeled as a harmonic current source for Steady-state and Time-domain simulations.
- o **Use harmonic model for frequency-scan simulations:** If this option is checked, the Fundamental frequency current magnitude input and the first line of the Harmonic data table are adjusted to match the Load-Flow solution current.
- o
- o **Adjust fundamental frequency current to match Load-Flow solution results:** If this option is checked, this device is modeled as a harmonic current source during Frequency scan simulations
- o **Fundamental frequency current magnitude (for one inverter)**: Magnitude of the fundamental frequency current for 1 inverter in A RMS. This value is automatically multiplied by the number of inverters in service.
- o **Harmonics data table:** Harmonic contents [harmonic number, I mag(%), I Angle (deg), Z(Ohm), Z Angle(deg)] for phase A (balanced source)

3 Inverter device model

3.1 General

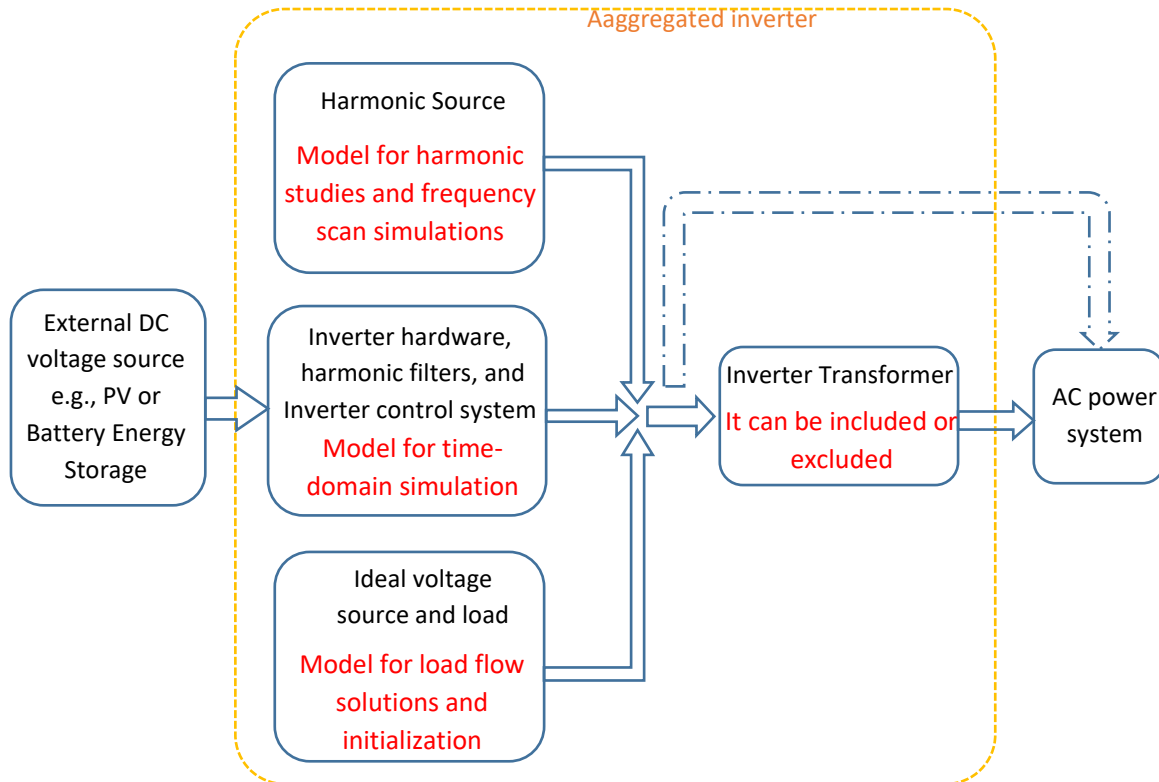The general structure of the converter model is shown in Figure 1.

Figure 1   General structure of three-phase GFM inverter model

The inverter subcircuit is automatically modified according to the simulation type, so the model is valid for any simulation options EMTP® offers.

During load-flow, the inverter is modelled by a PV bus or Slack bus. The load-flow power is the *Initial active power* input, and the voltage amplitude is the *Initial voltage input*.

In time-domain, the model is initialized with the load-flow conditions and the outer loop control (primary control) initial references are the ones used during load-flow, which were detailed in the section hereabove. The initialization time is t_init =0.05s. During this time, an ideal voltage source is connected to the inverter 3-phase pin. This voltage source holds the load-flow conditions while the inverter controls are initializing. After this time, the ideal voltage source is disconnected by a switch.

The active power, reactive power and voltage references may be dynamically varied by changing reference inputs (Pref, Qref, and Vacref) inside the "refs" bundle of the device. See here how to use bundle.
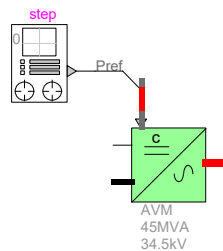
These inputs may either be:

- deviations from the initial references, in which case, they may be set to 0 to maintain load-flow condition in time-domain. The *Use power reference changes for input* option may be checked to enable this option.
- references, in which case, the actual reference value of the outer control loops may be set as inputs.

If an input is set to zero or is not connected, it is assumed to be 0. The inputs are in per unit.

During frequency-scan analysis, the converter is a Norton harmonic source. It is connected to the low-voltage side of the converter transformer if the latter is included. No control is included when the harmonic representation is selected.

3.2 Converter Modeling

Figure 2 shows the GFM inverter model.

GFM_inverter2

AVM
45MVA
34.5kV
VSM based GFM
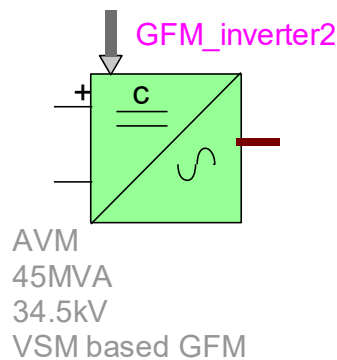
Figure 2   GFM Inverter model

As shown in Figure 3, the GFM inverter model is composed of

- "Inverter hardware" block

- "Inverter Control System" block,

- Inverter transformer (or converter transformer),

- PV/Slack initialization block

- Harmonics block which is a Norton harmonic source for harmonic analysis.

The PV/Slack initialization source contains a load-flow device and an ideal voltage source. It provides a flat start condition during initialization of inverter electrical and control systems.
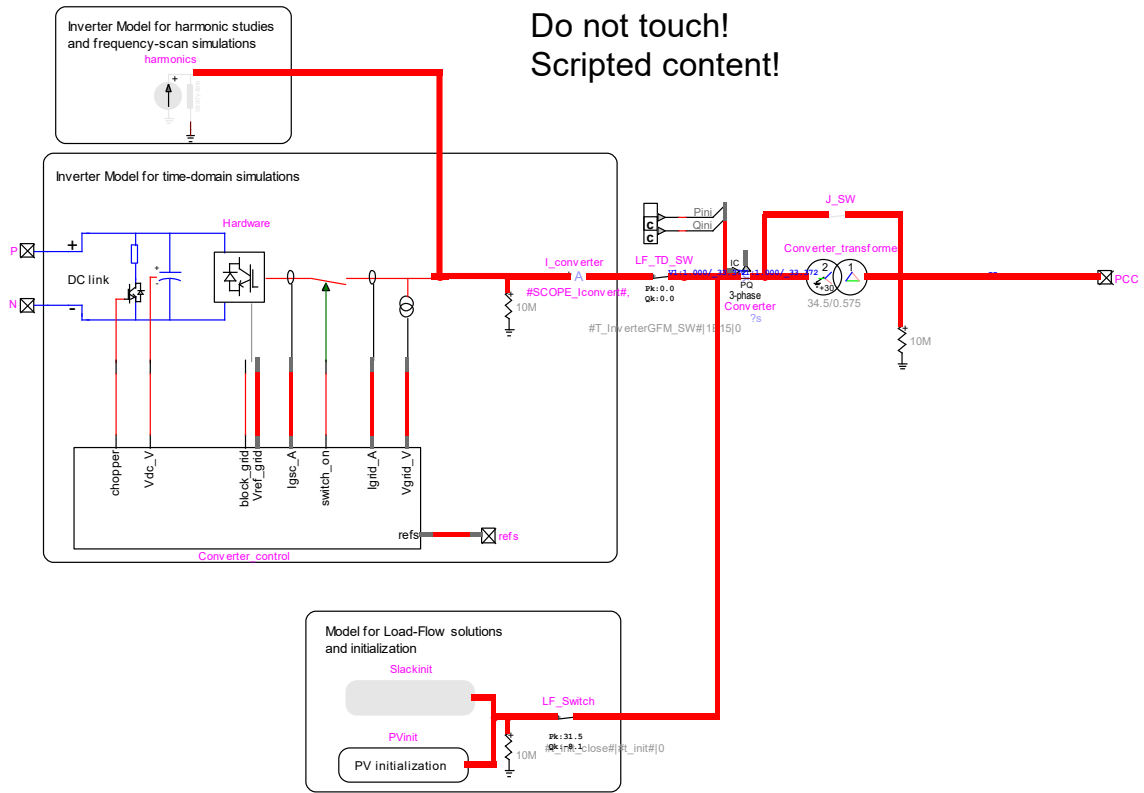
Figure 3   EMTP diagram of the GFM Inverter model

3.3 Hardware

Figure 4 shows the inverter hardware in EMTP. The inverter hardware is composed of a DC-AC converter, a series RL branch (choke filter), two shunt AC harmonic filters, and the current and voltage measurement units used for monitoring and control purposes. All variables are monitored as instantaneous values and meter locations are shown in Figure 4. The DC-AC converter model can be detailed model or average value model. The DC resistive chopper limits the DC bus voltage and is controlled by the protection system block. This option is used when the DC bus is connected to PV or battery systems.
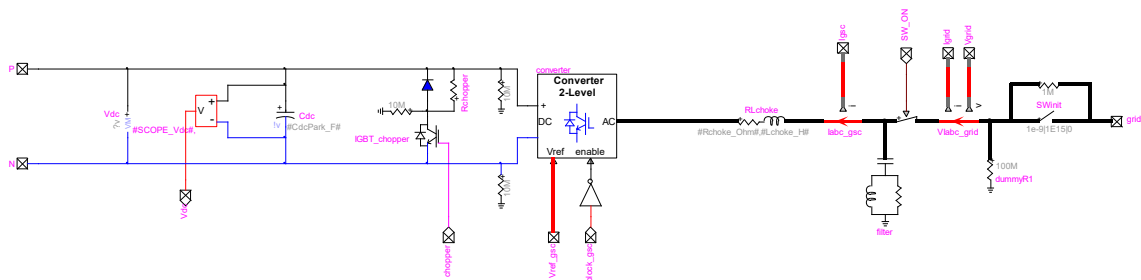
Figure 4   Inverter hardware

3.4 DC-AC converter model: detailed model (DM) and average value model (AVM)

The EMTP diagram of the detailed model (DM) is shown in Figure 5. It includes a two-level voltage source converter (VSC) block and a pulse width modulation (PWM) block.

A detailed two-level topology (Figure 6.a) is used for the VSC in which the valve is composed by one IGBT switch, two non-ideal (series and anti-parallel) diodes and a snubber circuit as shown in Figure 6.b. The non-ideal diodes are modeled as non-linear resistances.

The PWM block receives the three-phase reference voltages from converter control and generates the pulse pattern for the six IGBT switches by comparing the voltage reference with a triangular carrier wave. In a two-level converter, if the reference voltage is higher than the carrier wave then the phase terminal is connected to the positive DC terminal, and if it is lower, the phase terminal is connected to the negative DC terminal. The EMTP diagram of the PWM block is presented in Figure 7.
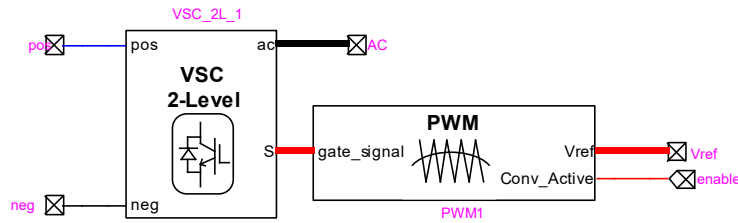

Figure 5   DC-AC converter block inside the inverter hardware model (detailed model version)
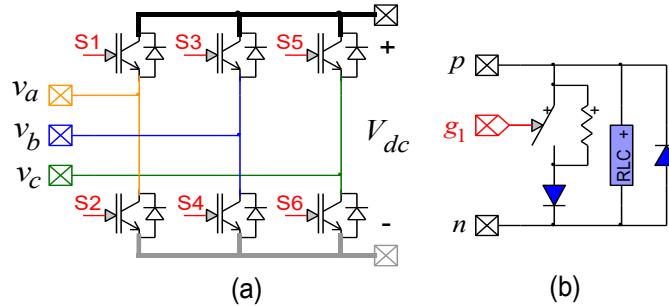

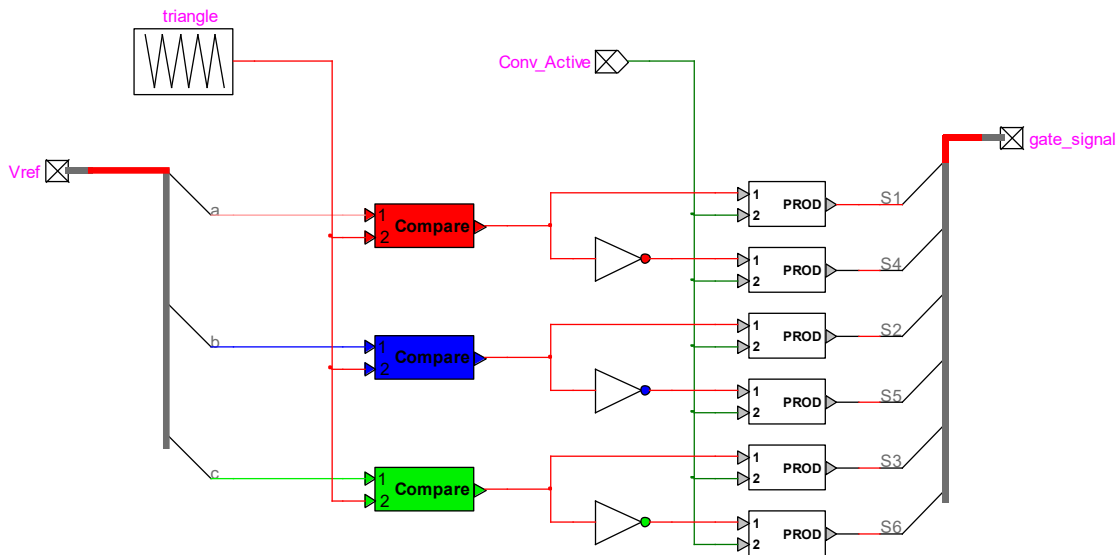Figure 6   (a) Two-level Converter, (b) IGBT valve

Figure 7   PWM control block

The DM mimics the converter behavior accurately. However, simulation of such switching circuits with variable topology requires many time-consuming mathematical operations and the high frequency PWM signals force small simulation time step usage. These computational inefficiencies can be eliminated by using average value model (AVM) which replicates the average response of switching devices, converters and controls through simplified functions and controlled sources [5] AVMs have been successfully developed for inverter-based technologies [6]. AVM obtained by replacing DM of converters with voltage-controlled sources on the AC side and current-controlled sources on the DC side as shown in Figure 8.

The fourth (converter control) tab of the inverter device mask (see 2.2) enables used AVM-DM selection.
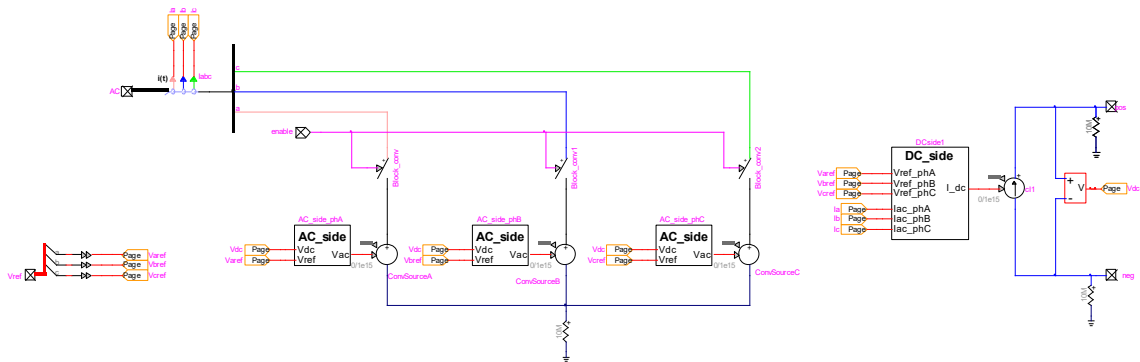

Figure 8   AVM Representation of the VSC

3.4.1 Shunt AC harmonic filters

The "shunt AC harmonic filters" block includes two harmonic filters as shown in Figure 9. These filters are tuned at switching frequencies harmonics n1 and n2 [7]. The filter parameters are computed as

$$C_{f1} = \frac{Q_{filter} \; N_{Inv}}{U^2 (2\pi f)} \tag{1}$$

$$L_{f1} = \frac{N_{Inv}}{C_{f1}(2\pi f n_1)^2} \tag{2}$$

$$R_{f1} = \frac{(2\pi f)n_1 \; L_{f1} \; Q}{N_{Inv}} \tag{3}$$

$$C_{f2} = C_{f1} \tag{4}$$

$$L_{f2} = \frac{N_{Inv}}{C_{f2}(2\pi f n_2)^2} \tag{5}$$

$$R_{f2} = \frac{(2\pi f)n_2 \; L_{f2} \; Q}{N_{Inv}} \tag{6}$$

where U is the rated LV grid voltage, Q_{filter} is the reactive power of the filter for one inverter, Q is the quality factor, and N_{Inv} is the number of the parallel inverters. Q_{filter} is set from the inverter mask (see 2.2). The switching frequencies harmonics n1 and n2 are as follows

$$n_1 = \frac{f_{PWM}}{f_s} \tag{7}$$

$$n_2 = 2n_1 \tag{8}$$

where f_{PWM} is the PWM frequency and f_s is the nominal frequency.

In case another type of filter (LC or LCL filter) or other parameters may be used, the filter can be modified by the user inside the inverter subcircuit. If several inverters are found in the network, the filter subcircuit and its parents must be made unique to avoid modifying all inverters instances.
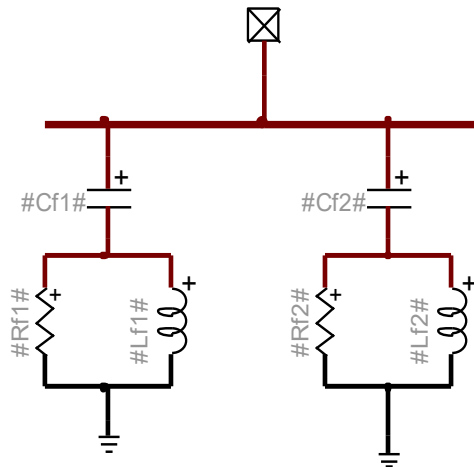

Figure 9   "shunt ac harmonic filter" block

3.5 GFM Inverter control system

The EMTP diagram of the inverter control system block is shown in Figure 10. The sampled signals are converted to pu and filtered. The sampling frequency can be modified by the user from the device mask (see 2.2). The "sampling" blocks are deactivated in AVM due to large simulation time step usage. Low pass filters (LPFs) are used for rejecting high frequency signals. The cut-off frequencies of the filters can be modified by the user from the inverter device mask (see 2.2). In this version, first-order LPFs are used. The protection block includes the AC over/under voltage protections, deep voltage sag detector, the DC chopper control, and overcurrent detector.
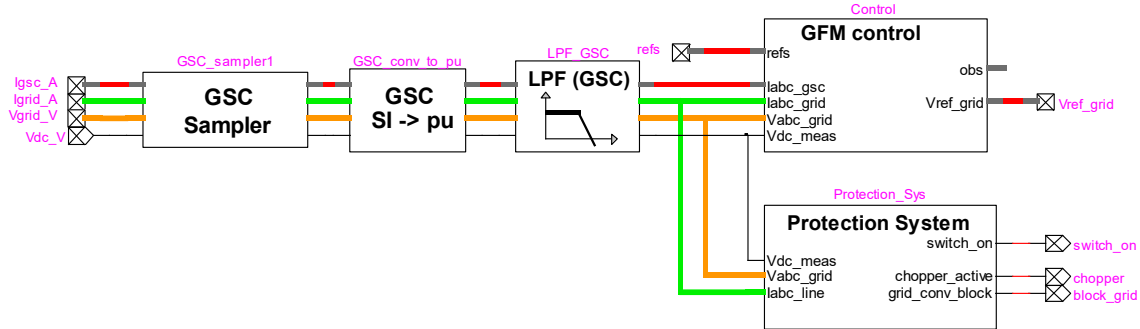

Figure 10   EMTP diagram of the GFM inverter control block

3.5.1 Inverter control

The EMTP diagram of the "GFM Control" block is shown in Figure 11. It includes reference, inverter computing variables, primary control (droop, VSM, and dVOC controls), and inner control (voltage and current controls) blocks.

The "Inverter Computing Variables" block does the dq transformation required for the vector control. The Park transformation matrix transforms abc-frame waveforms into dq-frame components rotating at synchronous reference angle $\theta = \int \omega$. The synchronous reference speed ω is sent from the primary control. A synchronous reference frame (SRF) PLL is also used in this block to monitor and measure the grid frequency [7].

The "Primary control" block with dynamics may be based on droop, VSM, or dVOC control methods, generates voltage and frequency (angle) references for the inner voltage and current controls (see 3.5.1.2). If the PLL-based GFM is selected, the "Primary control" block generates the voltage (Vd) reference and active power error references to the inner control (see 3.5.1.2).

The "inner control" block regulates the voltage, active power and current of the inverter using proportional integral (PI) controllers. It generates voltage references in the abc-frame for the inverter. The design approach for the inner current control is explained in [7].
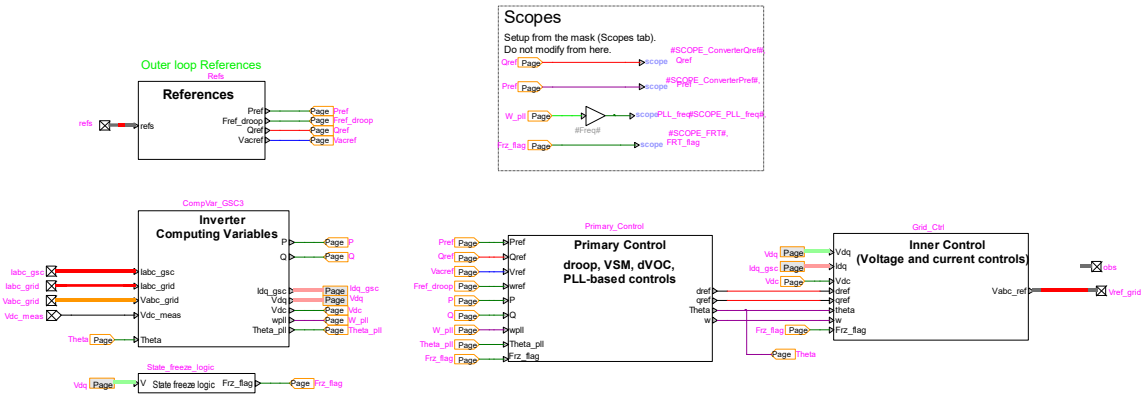
Figure 11   EMTP diagram of "GFM inverter control" block

3.5.1.1 Inner current and voltage loop controls

The voltage & active power control, the idq reference limiter and the current control diagrams are shown in Figure 12.

The voltage & active power control is implemented as a PI controller. It generates current references in dq-frame by comparing the voltage reference and voltage grid in the dq-frame. Figure 13 shows the inside of the voltage control block.

An inner current control loop and current reference limiter are used to control the output current of the inverter and limit its value to a desired range of values, which are based on the inverter ratings. The dynamic modeling of the current loop is explained in [7]. "Idq reference limiter" is used to limit the current references based on priority of the active current or reactive current.
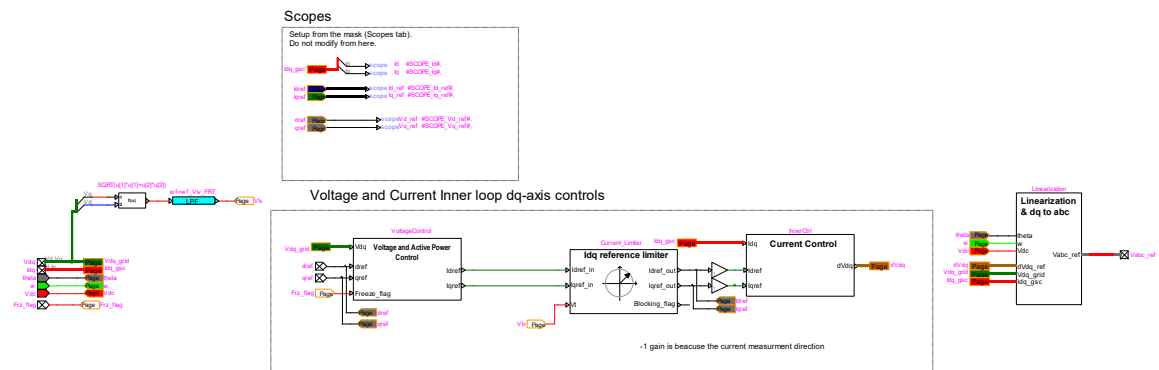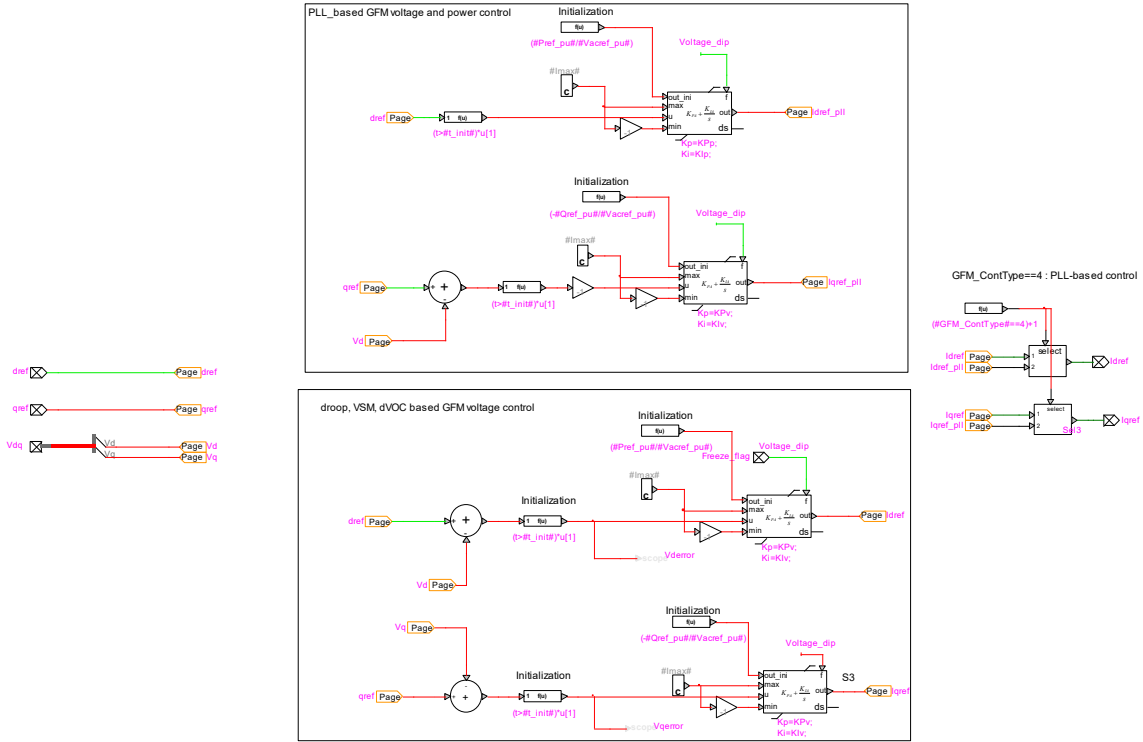

Figure 12   EMTP diagram of "inner control" block

Figure 13   EMTP diagram of "Voltage and active power control" block

3.5.1.2 Primary control

The primary control modeling approach for droop-based, VSM-based and dVOC-based GFM inverters is based on a generic primary-control model for grid-forming inverters presented in [2]. The dynamics of the generic model are described as:

$$\tau_f \frac{d\omega}{dt} = -\omega + \omega_0 + k_d(\omega_g - \omega) + k_f(p_{ref} - p_m) \tag{1}$$

$$\tau_v \frac{dV}{dt} = f_v(V) + k_v(q_{ref} - q_m) \tag{2}$$

$$\tau_p \begin{bmatrix} \dfrac{dp_m}{dt} \\ \dfrac{dq_m}{dt} \end{bmatrix} = -\begin{bmatrix} p_m \\ q_m \end{bmatrix} + \begin{bmatrix} p \\ q \end{bmatrix} \tag{3}$$

where ω is the inverter angular frequency,

ω_0 is nominal angular frequency,

ω_g is the grid angular frequency measured by PLL,

V is the inverter voltage magnitude,

V_0 is the nominal voltage magnitude,

p is measured active power output of the inverter,

q is measured active power output of the inverter,

p_{ref} is reference active power output of the inverter, and

q_{ref} is reference reactive power output of the inverter.

τ_f, k_d, k_f, τ_v, k_v, τ_p and $f_v(V)$ are dependent parameters which are changed according to GFM control strategy, as described in Table **2**. The parameters of Table **2** are defined at the device mask (see 2.2).

The PLL-based GFM inverter model is presented in [4]. The frequency and voltage droop gains for the PLL-based GFM in EMTP are set based on Table **2**.

Figure 14 shows the primary control model in EMTP.

For all control modes, the inverter can limit active and reactive powers at the inverter level (see 2.2), in addition to the current limits.

Table 2 dependent parameters under which the GFM transforms to droop, VSM, dVOC and PLL-based controls

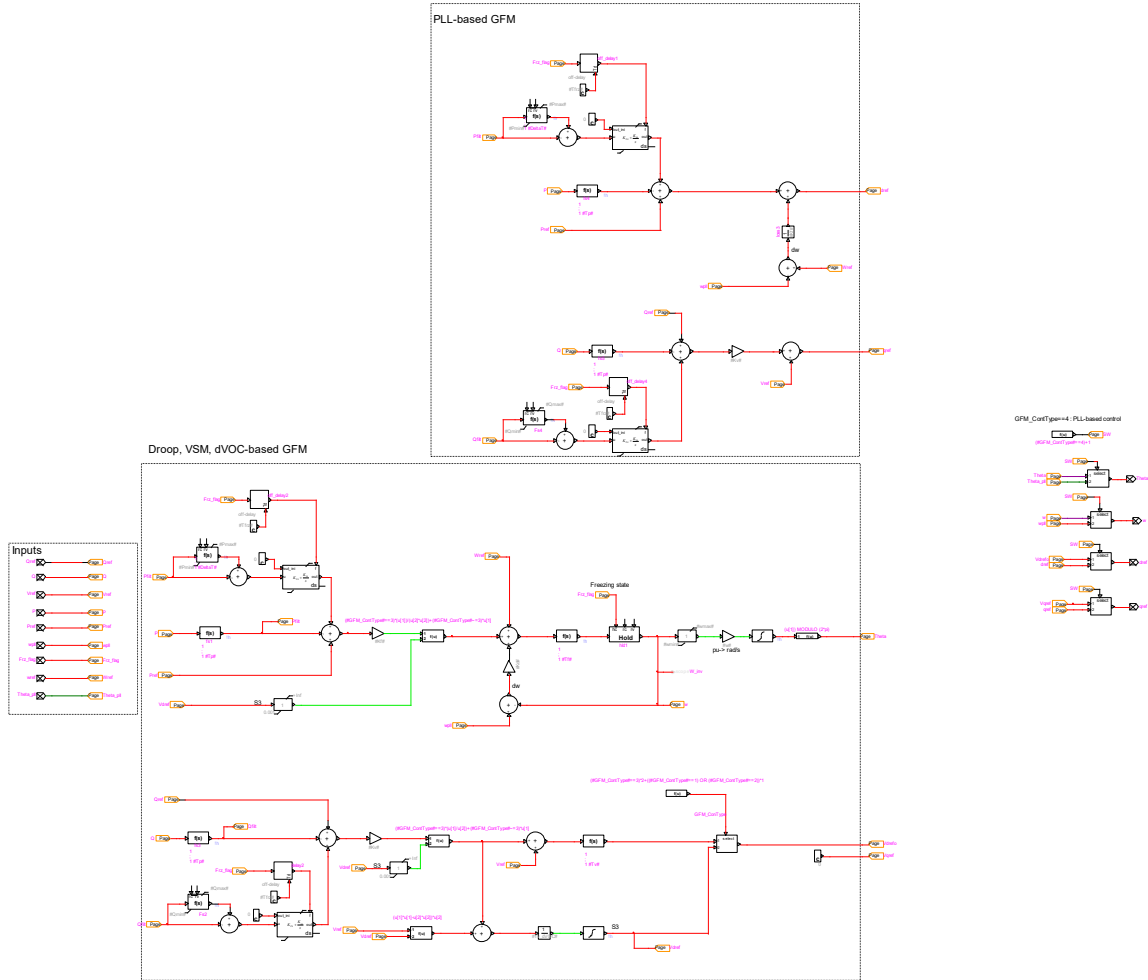|	τ_f	τ_v	τ_p	k_d	k_f	k_v	$f_v(V)$	Equations
PLL-based	NA	NA	$\dfrac{1}{\omega_c}$	NA	$\dfrac{1}{d_f}$	$\dfrac{1}{d_v}$	NA	$P_{oref} = d_f(\omega_g - \omega) + (p_{ref} - p_m)$ $V = V_0 + \dfrac{1}{d_v}(q_{ref} - q_m)$
droop	0	0	$\dfrac{1}{\omega_c}$	0	$\dfrac{1}{d_f}$	$\dfrac{1}{d_v}$	$-V + V_0$	$\omega = \omega_0 + \dfrac{1}{d_f}(p_{ref} - p_m)$ $V = V_0 + \dfrac{1}{d_v}(q_{ref} - q_m)$
VSM	$\dfrac{m_f}{d_f}$	0	$\dfrac{1}{\omega_c}$	$\dfrac{d_d}{d_f}$	$\dfrac{1}{d_f}$	$\dfrac{1}{d_v}$	$-V + V_0$	$\dfrac{m_f}{d_f}\dfrac{d\omega}{dt} = -\omega + \omega_0 + \dfrac{d_d}{d_f}(\omega_g - \omega)$ $\qquad + \dfrac{1}{d_f}(p_{ref} - p_m)$ $V = V_0 + \dfrac{1}{d_v}(q_{ref} - q_m)$
dVOC	0	$\dfrac{1}{\omega_0}$	0	0	$\dfrac{\omega_0 k_1}{V^2}$	$\dfrac{k_1}{V}$	$k_2(-V^3 + V_0^2 V)$	$\omega = \omega_0 + \dfrac{\omega_0 k_1}{V^2}(p_{ref} - p_m)$ $\dfrac{1}{\omega_0}\dfrac{dV}{dt} = k_2(-V^3 + V_0^2 V)$ $\qquad + \dfrac{k_1}{V}(q_{ref} - q_m)$

Figure 14　　　　Primary control model

3.6 Inverter protection system block

The "protection system" block includes an over/under voltage relay, deep voltage sag detector, dc overvoltage protection and an overcurrent detector for each converter to protect IGBT devices when the system is subjected to overcurrent. For initialization, all protection systems, except for DC chopper protection, are activated after 300ms of simulation (i.e. init_Prot_delay = 0.3s). The protection system parameters (except over/under voltage relay) can be modified from the device mask as shown in 2.2.

3.6.1 Over/under voltage protections and deep voltage sag detector

The over/under voltage protections are designed based on the technical requirements set by Hydro Quebec for the integration of renewable generation. The over/under voltage limits as a function of time is presented in Figure 15 and can be modified in the inverter device mask. The voltages below the red line reference and above the black line reference correspond to the ride-through region where the inverter is supposed to remain connected to the grid.
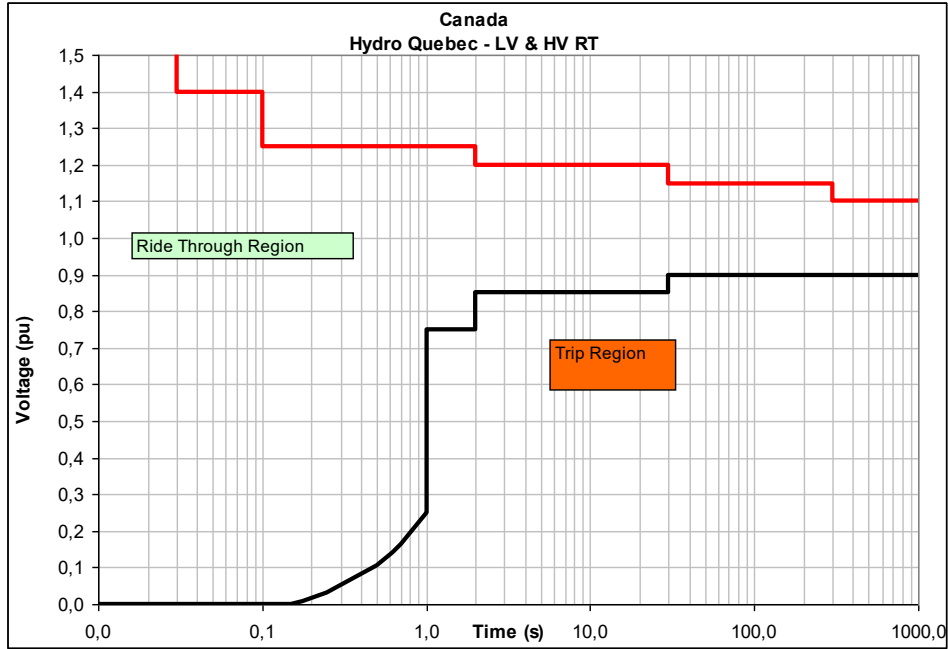
Figure 15   LVRT and HVRT requirements [8]

This block measures the rms voltages on each phase and sends a trip signal to the inverter circuit breaker when any of the phase rms voltage violates the limits in Figure 15 (see the upper part of Figure 16).

The "Deep Voltage Sag Detector" block (lower part of Figure 16) temporary blocks the Inverter in order to prevent potential overcurrent and restrict the FRT operation to the faults that occur outside the inverter.
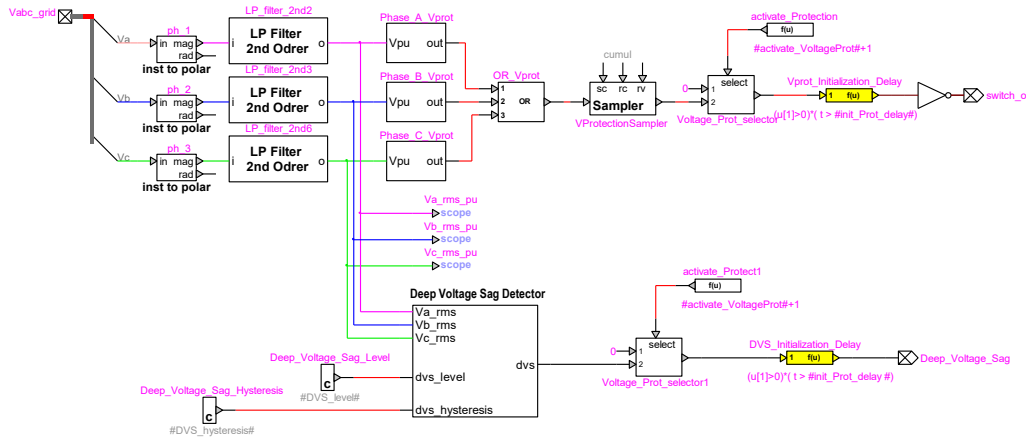

Figure 16   Over/under-voltage protections and deep voltage sag protection

3.6.2 DC overvoltage protection block

The function of DC chopper is to limit the DC bus voltage. It is activated when the dc bus voltage exceeds $\left|U_{chopper-ON}\right|$ and deactivated when dc bus reduces below $\left|U_{chopper-OFF}\right|$. EMTP diagram of the "dc overvoltage protection" is shown in Figure 17.
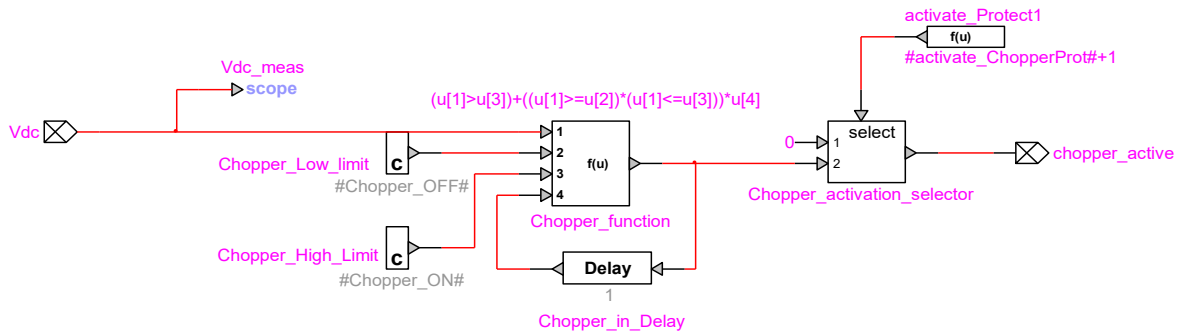
Figure 17   dc overvoltage protection block

3.6.3 overcurrent protection block

The overcurrent protection shown in Figure 18 blocks the converter temporarily when the converter current exceeds the pre-specified limit.
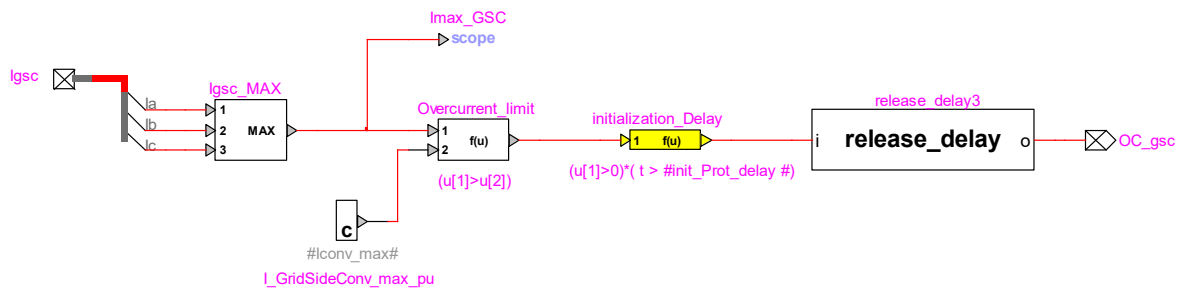

Figure 18   Overcurrent protection block

3.7 Inverter harmonic model

For harmonic analysis, the PV park is modeled with a harmonic Norton source. The harmonic study can be done in time domain, in which case **Use harmonic model for steady-state and time-domain simulations** must be checked or in the frequency domain with the frequency-scan simulation option, in which case **Use harmonic model for frequency-scan simulations**.

The harmonic currents are provided in percentage of the fundamental, for one inverter. The total park current is rescaled according to the number of inverters in service.

It is possible to automatically adjust the fundamental frequency current generated by each inverter and the harmonic current angles to match the load-flow results by checking Adjust fundamental frequency current to match Load-Flow results. When this box is checked, the I Angle input of the first line, which corresponds to the fundamental frequency current is adjusted to match the inverter current angle during the load-flow. The Fundamental frequency current magnitude is also adjusted to match the load-flow results. The fundamental frequency angle value is also added to the I Angle values of the other harmonics. Therefore, when this option is checked, the phase difference between the harmonic currents and the fundamental frequency current should be entered in the **I Angle** column.

4 Inverter Model Simulations

In this section, some simulation results are presented to demonstrate some features of the GFM inverter. Figure 19 shows the setup of the network used for simulations. The initial voltage and active power of the GFM are respectively set to 1.02pu and 0.7pu. The initial active and reactive power of the grid-following inverter (GFL) are respectively set to 0.7pu and 0. The rated power for both GFM and GFL inverters is 45MW. The short-circuit power of the external grid is 500MVA at 34.5kV.

Several events are defined during the simulation.

- At t=1s, the breaker connecting the external grid to the rest of the circuit is opened, and both GFL and GFM inverters supply the load thereby making a 100% inverter network.
- At t=1.5s a 10MW, 10MVAR load is connected to the network and then it is disconnected at t=2s.
- At t=2.8s a three-phase fault occurs at Bus 1 and the fault clears at 3s.

Figure 20 to Figure 23 show the simulation results when the GFM inverter is set to droop-base, VSM, dVOC, and PLL-based control respectively. The GFM inverter can regulate its active and reactive power output by controlling the voltage amplitude and frequency.
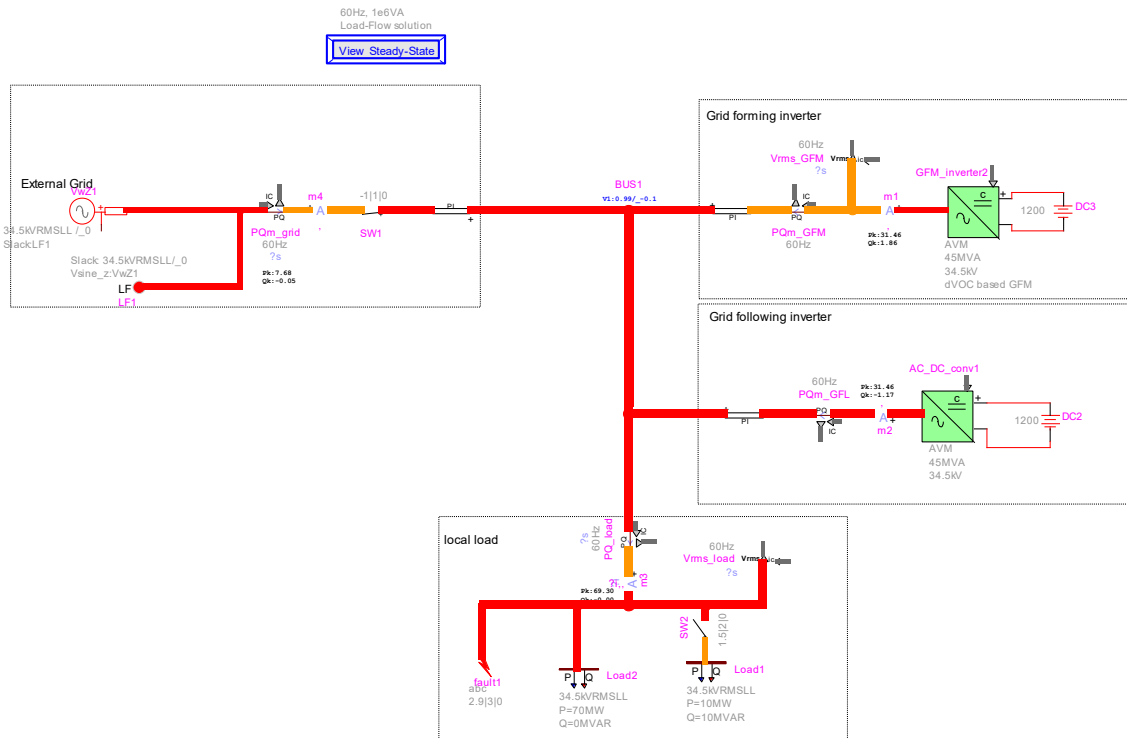

Figure 19   Initialization and flat start test: inverter active and reactive power
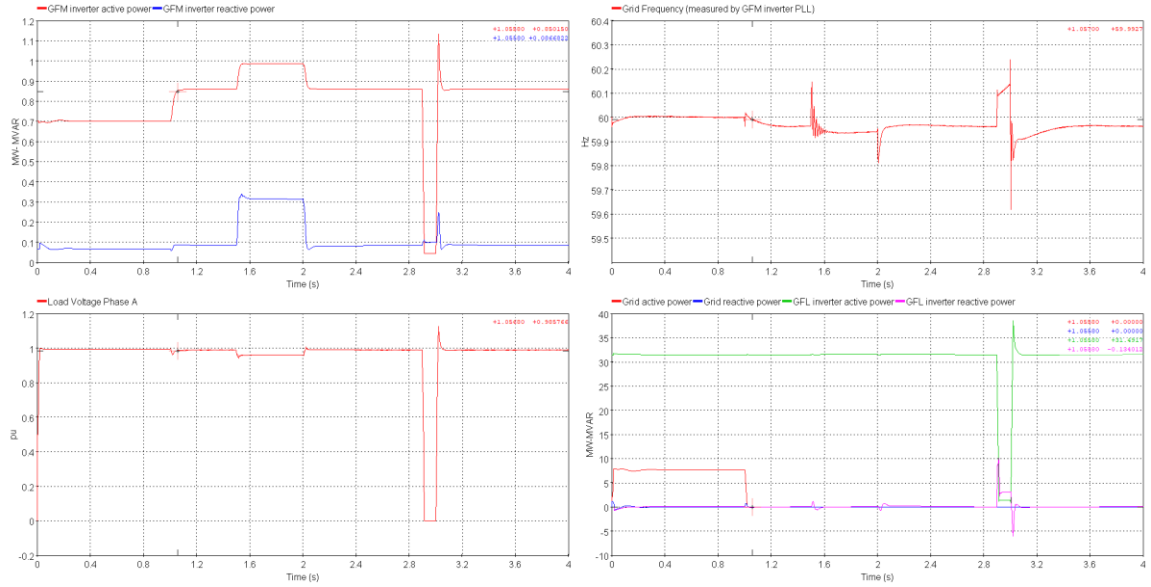
Figure 20   Simulation results when GFM inverter is set to droop-based control
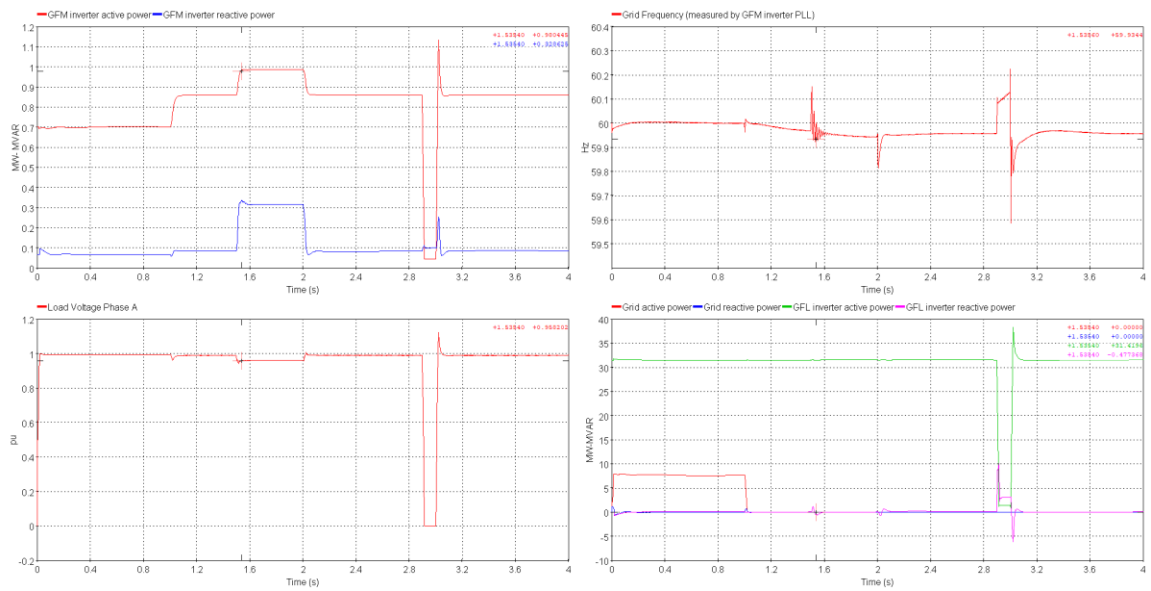

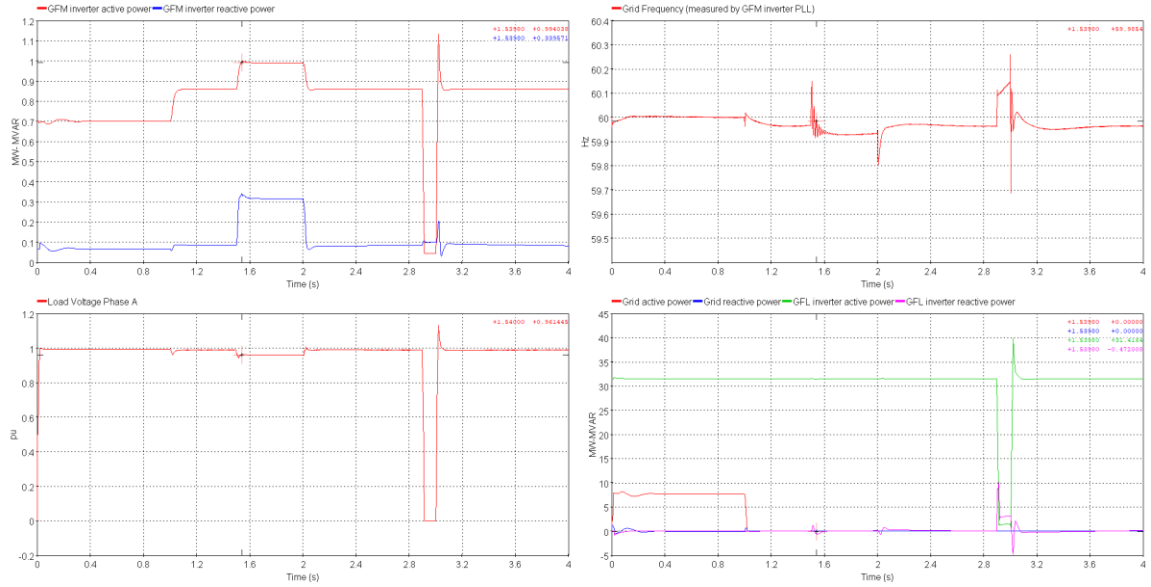Figure 21   Simulation results when GFM inverter is set to VSM control

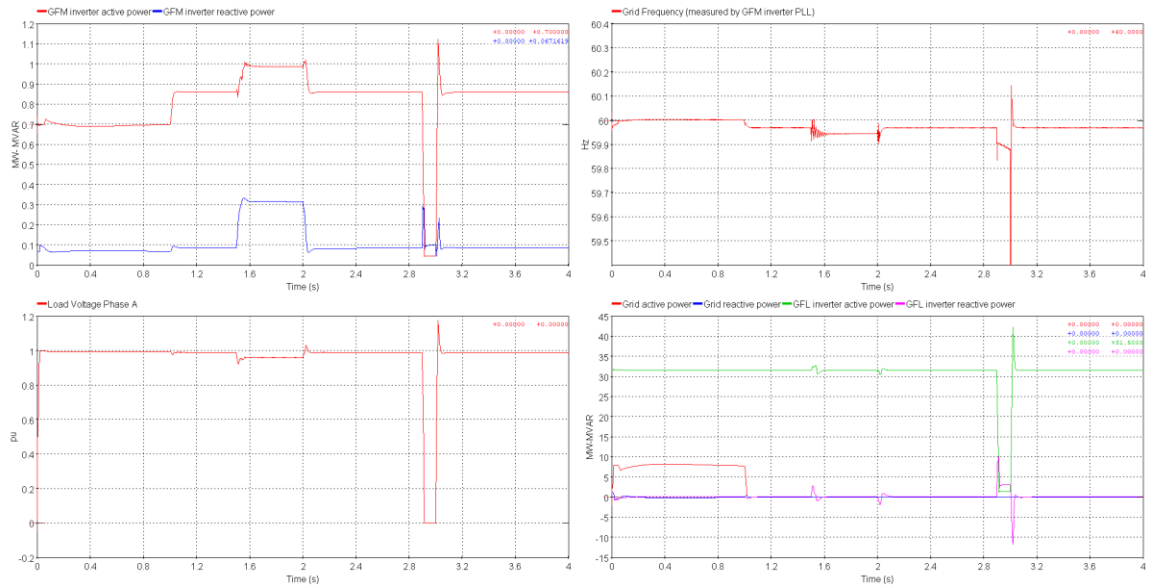Figure 22   Simulation results when GFM inverter is set to dVOC control

Figure 23   Simulation results when GFM inverter is set to PLL-based control

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