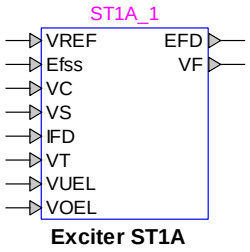
Exciters and Governors: Exciter ST1A



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1 Description

This device is an implementation of an IEEE type ST1A excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 10 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current	pu
VT	Input	Terminal voltage of synchronous machine	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
EFD	Output	The field voltage signal	pu
VF	Output	The excitation system stabilizer signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_A**: voltage regulator gain

2. **Time constant T_A**: voltage regulator time constant
3. **Maximum regulator output V_{Imax}**: maximum regulator voltage input
4. **Minimum regulator output V_{Imin}**: minimum regulator voltage input
5. **Maximum regulator output V_{Amax}**: maximum regulator voltage output
6. **Minimum regulator output V_{Amin}**: minimum regulator voltage output
7. **Maximum regulator output V_{Rmax}**: maximum regulator voltage output
8. **Minimum regulator output V_{Rmin}**: minimum regulator voltage output
9. **Time constant T_B**: time constant of the lead-lag compensator
10. **Time constant T_C**: time constant of the lead-lag compensator
11. **Time constant T_{B1}**: time constant of the lead-lag compensator
12. **Time constant T_{C1}**: time constant of the lead-lag compensator
13. **Gain K_F**: excitation control system stabilizer gain
14. **Time constant T_F**: excitation control system stabilizer time constant
15. Under Excitation Limiter option: see explanations below.
16. Over Excitation Limiter option: see explanations below.
17. Power System Stabilizer option: see explanations below.

There are three possible selections for the Under Excitation Limiter option:
1. VUEL not available or added to the reference voltage
2. VUEL connected to the first high value gate (HV gate)
3. VUEL connected to the second high value gate (HV gate)

There are two possible selections for the Over Excitation Limiter option:
1. VOEL not available
2. VOEL connected to the low value gate (LV gate)

There are two possible selections for the Power System Stabilizer option:
1. VS added to the reference voltage
2. VS added to the regulator output

1.2.2 Exciter tab

The exciter tab allows to input:
1. **Gain K_{LR}**: exciter output current limiter gain
2. **Current limiter reference I_{LR}**: exciter output current limiter reference
3. **Rectifier loading factor K_C**: rectifier loading factor

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2005.