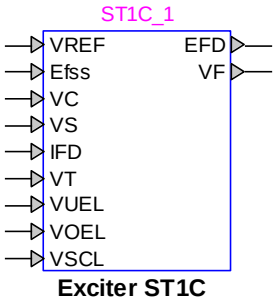
Exciters and Governors: Exciter ST1C



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1 Description

This device is an implementation of an IEEE type ST1C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 11 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current	pu
VT	Input	Terminal voltage of synchronous machine	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	The field voltage signal	pu
VF	Output	The excitation system stabilizer signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_A**: Voltage regulator gain
2. **Time constant T_A**: Voltage regulator time constant
3. **Maximum regulator input V_{Imax}**: Maximum voltage error (regulator input)
4. **Minimum regulator input V_{Imin}**: Minimum voltage error (regulator input)
5. **Maximum regulator output V_{Amax}**: Maximum regulator voltage output
6. **Minimum regulator output V_{Amin}**: Minimum regulator voltage output
7. **Maximum exciter output V_{Rmax}**: Maximum exciter output
8. **Minimum exciter output V_{Rmin}**: Minimum exciter output
9. **Time constant T_B**: Regulator denominator (lag) time constant
10. **Time constant T_C**: Regulator numerator (lead) time constant
11. **Time constant T_{B1}**: Regulator denominator (lag) time constant
12. **Time constant T_{C1}**: Regulator numerator (lead) time constant
13. **Gain K_F**: Rate feedback gain
14. **Time constant T_F**: Rate feedback time constant
15. **Under Excitation Limiter option**: see explanations below.
16. **Over Excitation Limiter option**: see explanations below.
17. **Stator Current Limiter option**: see explanations below.
18. **Power System Stabilizer option**: see explanations below.

There are three possible selections for the Under Excitation Limiter option:

1. VUEL not available or added to the reference voltage
2. VUEL connected to the first high value gate (HV gate)
3. VUEL connected to the second high value gate (HV gate)

There are three possible selections for the Over Excitation Limiter option:

1. VOEL not available or added to the reference voltage
2. VOEL connected to the first low value gate (LV gate)
3. VOEL connected to the first low value gate (LV gate)

There are five possible selections for the Stator Current Limiter option:

1. VSCL not available or added to the reference voltage: this option can be selected when the VSCL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VSCL connected to the first high value gate (HV gate).
3. VSCL connected to the first low value gate (LV gate).
4. VSCL connected to the second high value gate (HV gate).
5. VSCL connected to the second low value gate (LV gate).

There are two possible selections for the Power System Stabilizer option.

1. Vs connected to the reference voltage
2. Vs connected to the regulator output

1.2.2 Exciter tab

The parameters on the Exciter tab are:

1. **Gain K_{LR}**: Exciter output current limiter gain
2. **Current limiter reference I_{LR}**: Exciter output current limiter reference
3. **Rectifier loading factor K_C**: Rectifier loading factor proportional to commutating reactance

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value

must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] “IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies,” IEEE Standard 421.5-2016.