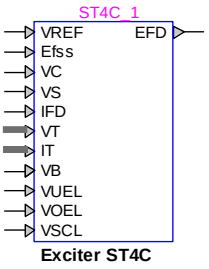
Exciters and Governors: Exciter ST4C



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1 Description

This device is an implementation of an IEEE type ST4C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 12 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current	pu
VT	Input, bundle	Terminal voltage (phasor) of synchronous machine (magnitude and phase)	pu
IT	Input, bundle	Current (phasor) of synchronous machine (magnitude and phase)	pu
VB	Input	Available exciter voltage	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	The field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_{PR}**: voltage regulator proportional gain
2. **Gain K_{IR}**: voltage regulator integral gain
3. **Time constant T_A**: thyristor bridge firing control equivalent time constant
4. **Maximum regulator output V_{Rmax}**: maximum regulator voltage output
5. **Minimum regulator output V_{Rmin}**: minimum regulator voltage output
6. **Gain K_{PM}**: forward proportional gain of inner loop field regulator
7. **Gain K_{IM}**: forward integral gain of inner loop field regulator
8. **Maximum field current output V_{Mmax}**: maximum field current output
9. **Minimum field current output V_{Mmin}**: minimum field current output
10. **Maximum exciter output V_{Amax}**: maximum exciter output
11. **Minimum exciter output V_{Amin}**: minimum exciter output
12. **Gain K_G**: feedback gain of field current regulator
13. **Time constant T_G:** feedback time constant of field current regulator
14. **Maximum feedback voltage V_{Gmax}**: maximum feedback voltage for the field current regulator
15. **Rectifier loading factor K_C**: rectifier loading factor proportional to commutating reactance
16. **Gain K_P**: potential circuit (voltage) gain coefficient
17. **Phase angle Theta$_P$**: potential circuit phase angle (degrees)
18. **Gain K_I**: compound circuit (current) gain coefficient
19. **Reactance X_L**: Reactance associated with potential source
20. **Field voltage V_{Bmax}**: maximum available exciter voltage
21. **Excitation Type option**: see explanations below.
22. **Under Excitation Limiter option**: see explanations below.
23. **Over Excitation Limiter option**: see explanations below.
24. **Stator Current Limiter option**: see explanations below.

There are two possible selections for the Excitation Type option:

1. Excitation system is self-excited: VT and IT inputs must be connected.
2. Excitation system comes from a separate source: VB input must be connected

There are three possible selections for the Under Excitation Limiter option:

1. VUEL is not available or added to the reference voltage
2. VUEL is connected to the first high value gate (HV Gate)
3. VUEL is connected to the second high value gate (HV Gate)

There are three possible selections for the Over Excitation Limiter option:

1. VOEL is not available or added to the reference voltage
2. VOEL is connected to the first low value gate (LV Gate)
3. VOEL is connected to the second low value gate (LV Gate)

There are five possible selections for the Stator Current Limiter option:

1. SCL is not available or added to the reference voltage
2. SCL is connected to the first high value gate (HV Gate)
3. SCL is connected to the first low value gate (LV Gate)
4. SCL is connected to the second high value gate (HV Gate)
5. SCL is connected to the second low value gate (LV Gate)

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] “IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies,” IEEE Standard 421.5-2016.