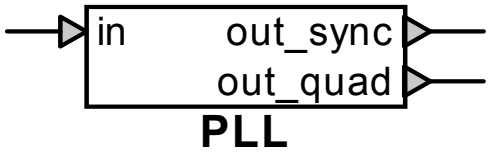
Control function: PLL



1 Description

This device is an implementation of a PLL (phase-locked loop) oscillator. The phase detector is a multiplier, and the loop filter is a first-order lag function with gain.

1.1 Pins

This device has three pins:

pin	*type*	*description*
in	input	input signal
out_sync	output	oscillator output, in phase with input
out_quad	output	oscillator output, in quadrature with input

1.2 Parameters

The following parameters must be defined:

parameter	*description*	*units*
freq	fundamental frequency	Hz
mag_ini	initial peak amplitude of input	units of input
Tc	filter time constant (lag)	s
Kc	filter gain	

1.3 Input

The input pin may be connected to any control signal.

1.4 Output

The outputs oscillate at the fundamental frequency of the input signal, and have a peak amplitude of 1. The output *out_sync* is in phase with the input signal, and *out_quad* in quadrature with the input signal. Their transient response is governed by the parameters Tc and Kc of the loop filter.

1.5 Representation

The implementation of the model can be inspected by opening the device's subcircuit.

The model represents a simple PLL. It uses a simple multiplier for detecting the phase error. A first-order transfer function with time constant Tc is used for filtering the error. The loop gain is Kc, and includes the sensitivity of the controlled oscillator. Taking into account the integrator, the loop is of order 2. The feedback (*out_quad*) is in quadrature with the input. An additional VCO is included to provide an output signal (*out_sync*) that is in phase with the input.