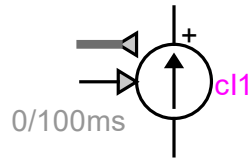


Controlled current source



Controlled current source	1
1 Description	1
1.1 Parameters	1
1.2 Netlist format	2
2 Steady-state model	2
3 Frequency Scan model	2
4 Time-domain model	2
4.1 Initialization	2

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1 Description

This device accepts only 1-phase signals.

1.1 Parameters

The device pins are:

- k the positive power pin
- m the negative power pin
- in the control input pin
- B1 the control output bundle (also called bus) pin that can contain observe signal pins

The model parameters are:

- t_{start} start time, if $t < t_{start}$ the source is an open-circuit.
- t_{stop} stop time, if $t > t_{stop}$ the source is an open-circuit. The stop time must be greater than the start time
- Extrapolate Extrapolation option (see below).

Since there is a time-step delay between the control signal setting and the electrical network solution with the determined current value, extrapolation can be used to compensate for this delay. Extrapolation allows to make a prediction based on previous solutions. The "Linear extrapolation" is applied using the previous solution points. The "Error correction" method simply predicts the solution using the previous time-point error.

1.2 Netlist format

```
_cl;c11;6;6;s1,s2,scontrol,bundle_v,bundle_i,bundle_p,
0,100ms,0,?v,?i,?p,>v,>i,>p,
```

Field	Description
<code>_cl</code>	Part name
<code>c11</code>	Instance name, any name.
<code>6</code>	Total number of pins
<code>6</code>	Number of pins given in this data section
<code>s1</code>	Signal name connected to k-pin (positive), any name
<code>s2</code>	Signal name connected to m-pin, any name
<code>scontrol</code>	Signal name connected to the control input pin
<code>bundle_v</code>	Signal name connected to the control output pin for observing voltage, optional
<code>bundle_i</code>	Signal name connected to the control output pin for observing current, optional
<code>bundle_p</code>	Signal name connected to the control output pin for observing power, optional
<code>t_start</code>	Start time
<code>t_stop</code>	Stop time
<code>extrapolate</code>	Extrapolation option: 0 means no extrapolation, 1 means Linear extrapolation, 2 means Error correction
<code>?v</code>	Request for voltage scope, sent to scope group vb (branch voltages), optional
<code>?i</code>	Request for current scope, sent to scope group ib (branch currents), optional
<code>?p</code>	Request for power scope, sent to scope group p (branch power), optional
<code>>v</code>	Request for voltage observe, optional
<code>>i</code>	Request for current observe, optional
<code>>p</code>	Request for power observe, optional

None of the device pins can be deleted.

2 Steady-state model

The steady-state model of this device is an open-circuit.

3 Frequency Scan model

The frequency scan model of this device is an open-circuit.

4 Time-domain model

The device output waveform is imposed by the control signal connected to its control input pin.

The source is active (not an open-circuit) for $t_{\text{start}} \leq t \leq t_{\text{stop}}$.

4.1 Initialization

It is feasible to provide automatic initial conditions using the steady-state solution option, by connecting a current source in parallel with the “I controlled” source. Such a source must be present during the steady-state solution and disconnected in the time-domain solution. In the example shown in Figure 1, the cosine current source (“I ac” device) has the desired steady-state waveform. In this demonstrative example it is the same as the waveform of the signal `cossig`. The `AC1` source start time is -1 (steady-state presence condition) and the stop time is 1e-15s. It is important to make the stop time much smaller than the integration time-step Δt . When the simulation starts all state-variables are in steady-state.

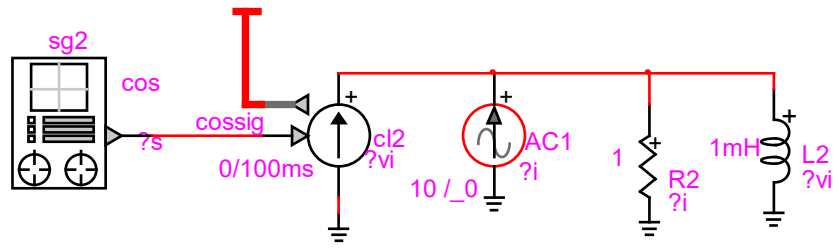


Figure 1 Automatic initialization example