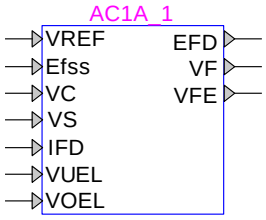
Exciters and Governors: Exciter AC1A



Exciter AC1A

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1 Description

This device is an implementation of the IEEE type AC1A excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 10 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
EFD	Output	The field voltage signal	pu
VF	Output	The excitation system stabilizer signal	pu
VFE	Output	Signal proportional to exciter field current	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_A**: voltage regulator gain

2. **Time constant T_A**: voltage regulator time constant
3. **Maximum regulator output V_{Amax}**: maximum regulator voltage output
4. **Minimum regulator output V_{Amin}**: minimum regulator voltage output
5. **Maximum regulator output V_{Rmax}**: maximum regulator voltage output
6. **Minimum regulator output V_{Rmin}**: minimum regulator voltage output
7. **Time constant T_B**: time constant of the lead-lag compensator
8. **Time constant T_C**: time constant of the lead-lag compensator
9. **Gain K_F**: excitation control system stabilizer gain
10. **Time constant T_F**: excitation control system stabilizer time constant
11. Under Excitation Limiter option: see explanations below.
12. Over Excitation Limiter option: see explanation below.

There are two possible selections for the Under Excitation Limiter option:
1. VUEL not available
2. VUEL connected to the high value gate (HV gate)

There are two possible selections for the Over Excitation Limiter option:
1. VOEL not available
2. VOEL connected to the low value gate (LV gate)

1.2.2 Exciter tab

The exciter tab allows to input:
1. **Gain K_E**: exciter gain
2. **Time constant T_E**: exciter time constant
3. **Demagnetizing factor K_D**: demagnetizing factor
4. **Rectifier loading factor K_C**: rectifier loading factor
5. **Voltage V_{E1}**: The exciter voltage point which is near the exciter ceiling voltage
6. **Voltage V_{E2}**: The exciter voltage point which is near 75% of V_{E1}
7. **Saturation function output SE_V_{E1}**: The exciter saturation function value at V_{E1}
8. **Saturation function output SE_V_{E2}**: The exciter saturation function value at V_{E2}

The exciter saturation function is defined as

$$S_E = A_{EX} e^{B_{EX} E_{FD}} \tag{1}$$

which gives the approximate saturation for any E_{FD} (exciter output voltage). According to [2] (see pages 562 and 563), the coefficients A_{EX} and B_{EX} can be found from:

$$A_{EX} = \frac{S_{V_{E2}}^4}{S_{V_{E1}}^3} \tag{2}$$

$$B_{EX} = \frac{4}{V_{E1}} \ln\left(\frac{S_{V_{E1}}}{S_{V_{E2}}}\right) \tag{3}$$

In the literature [2] $V_{E1} = V_{E_{max}}$ and $V_{E2} = V_{E_{0.75max}}$.

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] “IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies,” IEEE Standard 421.5-2005.

[2] P. M. Anderson and A. A. Fouad, “Power system control and stability”, second edition, IEEE Press, Wiley Interscience, 2003.