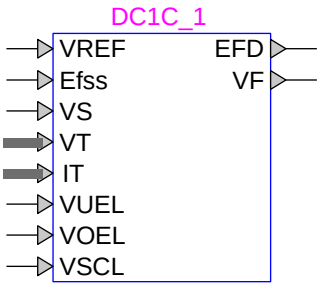
Exciters and Governors: Exciter DC1C



Exciter DC1C

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1 Description

This device is an implementation of the IEEE type DC1C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 7 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VS	Input	Power System Stabilizer signal	pu
VT	Input, bundle	Terminal voltage (phasor) of synchronous machine (magnitude and phase)	pu
IT	Input, bundle	Current (phasor) of synchronous machine (magnitude and phase)	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	The field voltage signal	pu
VF	Output	The excitation system stabilizer signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain X_C**: Resistive component of load compensation
2. **Gain R_C**: Reactance component of load compensation
3. **Time constant T_R**: Regulator input filter time constant
4. **Gain K_A**: Regulator output gain
5. **Time constant T_A**: Voltage regulator time constant
6. **Maximum regulator output V_{Rmax}**: Maximum regulator voltage output
7. **Minimum regulator output V_{Rmin}**: Minimum regulator voltage output
8. **Time constant T_B**: Regulator denominator (lag) time constant
9. **Time constant T_C**: Regulator numerator (lead) time constant
10. **Gain K_F**: Rate feedback gain
11. **Time constant T_F**: Rate feedback time constant
12. Under Excitation Limiter option: see explanations below.
13. Over Excitation Limiter option: see explanations below.
14. Stator Current Limiter option: see explanations below.

There are two possible selections for the Under Excitation Limiter option:

1. VUEL not available or added to the reference voltage: this option can be selected when the VUEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VUEL connected to the high value gate (HV gate)

There are two possible selections for the Over Excitation Limiter option:

1. VOEL not available or added to the reference voltage: this option can be selected when the VOEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VOEL connected to the low value gate (LV gate)

There are three possible selections for the Stator Current Limiter option:

1. VSCL not available or added to the reference voltage: this option can be selected when the VSCL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VSCL connected to the high value gate (HV gate).
3. VSCL connected to the low value gate (LV gate).

1.2.2 Exciter tab

The exciter tab allows to input:

1. **Gain K_E**: Exciter field proportional constant
2. **Time constant T_E**: Exciter field time constant
3. **Field voltage E_{FD1}**: The field exciter voltage point which is near the exciter ceiling voltage
4. **Field voltage E_{FD2}**: The field exciter voltage point which is near 75% of E_{FD1}
5. **Saturation function output SE_E_{FD1}**: The exciter saturation function value at E_{FD1}
6. **Saturation function output SE_E_{FD2}**: The exciter saturation function value at E_{FD2}

The exciter saturation function is defined as

$$S_E = A_{EX} e^{B_{EX} E_{FD}} \tag{1}$$

which gives the approximation saturation for any E_{FD} (exciter output voltage). According to [2] (see pages 562 and 563), the coefficients A_{EX} and B_{EX} can be found from:

$$A_{EX} = \frac{S_{E_{FD2}}^4}{S_{E_{FD1}}^3} \tag{2}$$

$$B_{EX} = \frac{4}{E_{FD1}} \ln\left(\frac{S_{E_{FD1}}}{S_{E_{FD2}}}\right) \quad (3)$$

In the literature [2] $E_{FD1} = E_{FD_{max}}$ and $E_{FD2} = E_{FD_{0.75max}}$.

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2016.

[2] P. M. Anderson and A. A. Fouad, "Power system control and stability", second edition, IEEE Press, Wiley Interscience, 2003.