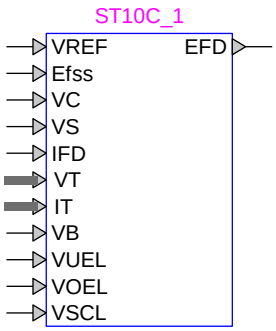
Exciters and Governors: Exciter ST10C



Exciter ST10C

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1 Description

This device is an implementation of the IEEE type ST10C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 12 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current signal	pu
VT	Input, bundle	Terminal voltage (phasor) of synchronous machine (magnitude and phase)	pu
IT	Input, bundle	Current (phasor) of synchronous machine (magnitude and phase)	pu
VB	Input	Available exciter voltage	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	Field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_R**: regulator gain
2. **Time constant T_{B1}**: voltage regulator denominator (lag) time constant 1
3. **Time constant T_{C1}**: voltage regulator numerator (lead) time constant 1
4. **Time constant T_{B2}**: voltage regulator denominator (lag) time constant 2
5. **Time constant T_{C2}**: voltage regulator numerator (lead) time constant 2
6. **Time constant T_{UB1}**: UEL regulator denominator (lag) time constant 1
7. **Time constant T_{UC1}**: UEL regulator numerator (lead) time constant 1
8. **Time constant T_{UB2}**: UEL regulator denominator (lag) time constant 2
9. **Time constant T_{UC2}**: UEL regulator numerator (lead) time constant 2
10. **Time constant T_{OB1}**: OEL regulator denominator (lag) time constant 1
11. **Time constant T_{OC1}**: OEL regulator numerator (lead) time constant 1
12. **Time constant T_{OB2}**: OEL regulator denominator (lag) time constant 2
13. **Time constant T_{OC2}**: OEL regulator numerator (lead) time constant 2
14. **Maximum PSS output V_{RSmax}**: maximum PSS regulator output
15. **Minimum PSS output V_{RSmin}**: minimum PSS regulator output
16. **Maximum output V_{Rmax}**: maximum regulator output
17. **Minimum output V_{Rmin}**: minimum regulator output
18. **Rectifier loading factor K_C**: rectifier loading factor proportional to commutating reactance
19. **Time constant T_1**: equivalent time constant for rectifier bridge
20. **Gain K_P**: potential circuit (voltage) gain coefficient
21. **Phase angle $Theta_P$**: potential circuit phase angle (degrees)
22. **Gain K_I**: potential circuit (current) gain coefficient
23. **Reactance X_L**: reactance associated with potential source
24. **Voltage V_{Bmax}**: maximum available exciter voltage
25. Excitation Type option: see explanations below.
26. Under Excitation Limiter option: see explanations below.
27. Over Excitation Limiter option: see explanations below.
28. Stator Current Limiter option: see explanations below.
29. Power System Stabilizer option: see explanations below.

There are two possible selections for the Excitation Type option:

1. Excitation system is self-excited: VT and IT inputs must be connected.
2. Excitation system comes from a separate source: VB input must be connected

There are three possible selections for the Under Excitation Limiter option:

1. VUEL not available or added to the reference voltage: this option can be selected when the VUEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VUEL connected to the first high value gate (HV gate).
3. VUEL connected to the second high value gate (HV gate).

There are three possible selections for the Over Excitation Limiter option:

1. VOEL not available or added to the reference voltage: this option can be selected when the VOEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VOEL connected to the first low value gate (LV gate).
3. VUEL connected to the second low value gate (LV gate).

There are five possible selections for the Stator Current Limiter option:

1. VSCL not available or added to the reference voltage: this option can be selected when the VSCL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VSCL connected to the first high value gate (HV gate).
3. VSCL connected to the first low value gate (LV gate).
4. VSCL connected to the second high value gate (HV gate).
5. VSCL connected to the second low value gate (LV gate).

There are three possible selections for the Power System Stabilizer option:

1. Vs not available or added to the reference voltage: this option can be selected when the Vs input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. Vs connected to the switch logic (SWLIM).
3. Vs connected to the second sum.

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] “IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies,” IEEE Standard 421.5-2016.