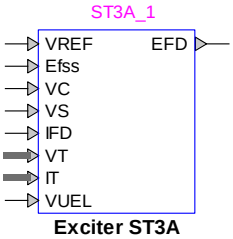
Exciters and Governors: Exciter ST3A



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1 Description

This device is an implementation of an IEEE type ST3A excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 9 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current	pu
VT	Input, bundle	Terminal voltage (phasor) of synchronous machine (magnitude and phase)	pu
IT	Input, bundle	Current (phasor) of synchronous machine (magnitude and phase)	pu
VUEL	Input	Under Excitation Limiter signal	pu
EFD	Output	The field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_A**: voltage regulator gain

2. **Time constant T_A**: thyristor bridge firing control time constant
3. **Time constant T_B**: lead-lag time constant
4. **Time constant T_C**: lead-lag time constant
5. **Maximum regulator input V_{Imax}**: maximum regulator voltage input
6. **Minimum regulator input V_{Imin}**: minimum regulator voltage input
7. **Maximum regulator output V_{Rmax}**: maximum regulator voltage output
8. **Minimum regulator output V_{Rmin}**: minimum regulator voltage output
9. **Gain K_G**: feedback gain of field current regulator
10. **Gain K_M**: forward gain of inner loop field regulator
11. **Gain T_M**: forward time constant of inner loop field regulator
12. **Voltage V_{Gmax}**: maximum field current feedback voltage
13. **Maximum field current output V_{Mmax}**: maximum output of field current regulator
14. **Minimum field current output V_{Mmin}**: minimum output of field current regulator
15. Under Excitation Limiter option: see explanations below.

There are two possible options for the Under Excitation Limiter option:

1. VUEL not available
2. VUEL connected to the high value gate (HV gate)

1.2.2 Exciter tab

The exciter tab allows to input:

1. **Gain K_P**: potential circuit (voltage) gain coefficient
2. **Phase angle Theta$_P$**: potential circuit phase angle (degrees)
3. **Gain K_I**: compound circuit (current) gain coefficient
4. **Rectifier loading factor K_C**: rectifier loading factor proportional to commutating reactance
5. **Field voltage V_{Bmax}**: maximum available exciter voltage
6. **Reactance X_L**: Reactance associated with potential source

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2005.