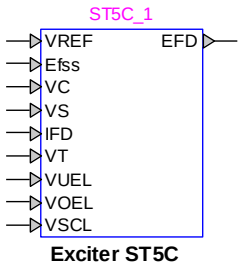
Exciters and Governors: Exciter ST5C



Hossein Ashourian, Jean Mahseredjian, 5/20/2021 11:19 PM

1 Description

This device is an implementation of an IEEE type ST5C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 10 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current	pu
VT	Input	Terminal voltage of synchronous machine (magnitude)	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	Field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Time constant T_{B1}**: voltage regulator time constant
2. **Time constant T_{C1}**: voltage regulator time constant
3. **Time constant T_{B2}**: voltage regulator time constant
4. **Time constant T_{C2}**: voltage regulator time constant
5. **Time constant T_{UB1}**: UEL time constant
6. **Time constant T_{UC1}**: UEL time constant
7. **Time constant T_{UB2}**: UEL time constant
8. **Time constant T_{UC2}**: UEL time constant
9. **Time constant T_{OB1}**: OEL time constant
10. **Time constant T_{OC1}**: OEL time constant
11. **Time constant T_{OB2}**: OEL time constant
12. **Time constant T_{OC2}**: OEL time constant
13. **Rectifier loading factor K_C**: rectifier loading factor proportional to commutating reactance
14. **Gain K_R**: voltage regulator gain
15. **Time constant T_1**: voltage regulator time constant
16. **Maximum regulator output V_{Rmax}**: maximum voltage regulator output
17. **Minimum regulator output V_{Rmin}**: minimum voltage regulator output
18. **Under Excitation Limiter option**: see explanations below.
19. **Over Excitation Limiter option**: see explanations below.
20. **Stator Current Limiter option**: see explanations below.

There are two possible options for the Under Excitation Limiter option:

1. VUEL is not available or added to the reference voltage (at voltage error
2. VUEL is connected to the high value gate (HV gate)

There are two possible options for the Over Excitation Limiter option:

1. VOEL is not available or added to the reference voltage (at voltage error)
2. VOEL is connected to the low value gate (LV gate)

There are three possible options for the Stator Current Limiter option:

1. V_{SCL} is not available or added to the reference voltage
2. V_{SCL} is connected to the high value gate (HV Gate)
3. V_{SCL} is connected to the low value gate (LV Gate)

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2016.