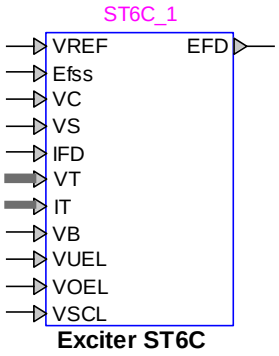
Exciters and Governors: Exciter ST6C



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1 Description

This device is an implementation of the IEEE type ST6C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 12 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current signal	pu
VT	Input, bundle	Terminal voltage (phasor) of synchronous machine (magnitude and phase)	pu
IT	Input, bundle	Current (phasor) of synchronous machine (magnitude and phase)	pu
VB	Input	Available exciter voltage	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	Field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_{PA}**: voltage regulator proportional gain
2. **Gain K_{IA}**: voltage regulator integral gain
3. **Gain K_{FF}**: pre-control gain inner loop field regulator
4. **Gain K_M**: forward gain inner loop field regulator
5. **Gain K_G**: feedback gain inner loop field regulator
6. **Time constant T_G**: feedback time constant inner loop field regulator
7. **Maximum voltage regulator output V_{Amax}**: maximum voltage regulator output
8. **Minimum voltage regulator output V_{Amin}**: minimum voltage regulator output
9. **Maximum regulator output V_{Rmax}**: maximum regulator output limit
10. **Minimum regulator output V_{Rmin}**: minimum regulator output limit
11. **Maximum rectifier output V_{Mmax}**: maximum rectifier output limit
12. **Minimum rectifier output V_{Mmin}**: minimum rectifier output limit
13. **Time constant T_A**: thyristor bridge firing control equivalent time constant
14. **Gain K_{LR}**: exciter output current limiter gain
15. **Current limit adjustment K_{CI}**: exciter output current limit adjustment
16. **Current limit reference I_{LR}**: exciter output current limit reference
17. **Rectifier loading factor K_C**: rectifier loading factor proportional to commutating reactance
18. **Gain K_P**: potential circuit gain coefficient
19. **Phase angle $Theta_P$**: potential circuit phase angle (degrees)
20. **Gain K_I**: compound circuit (current) gain coefficient
21. **Reactance X_L**: Reactance associated with potential source
22. **Field voltage V_{Bmax}**: maximum available exciter voltage
23. **Excitation Type option**: see explanations below.
24. **Under Excitation Limiter option**: see explanations below.
25. **Over Excitation Limiter option**: see explanations below.
26. **Stator Current Limiter option**: see explanations below.

There are two possible selections for the Excitation Type option:

1. Excitation system is self-excited: VT and IT inputs must be connected.
2. Excitation system comes from a separate source: VB input must be connected

There are four possible selections for the Under Excitation Limiter option:

1. VUEL is not available or added to the reference voltage (at voltage error)
2. VUEL is not available or added to the AVR input
3. VUEL is connected to the first high value gate (HV Gate)
4. VUEL is connected to the second high value gate (HV Gate)

There are four possible selections for the Over Excitation Limiter option:

1. VOEL is not available or added to the reference voltage (at voltage error)
2. VOEL is not available or added to the AVR input
3. VOEL is connected to the first low value gate (LV Gate)
4. VOEL is connected to the second low value gate (LV Gate)

There are six possible selections for the Stator Current Limiter option:

1. SCL is not available or added to the reference voltage
2. SCL is not available or added to the AVR input
3. SCL is connected to the first high value gate (HV Gate)
4. SCL is connected to the first low value gate (LV Gate)
5. SCL is connected to the second high value gate (HV Gate)
6. SCL is connected to the second low value gate (LV Gate)

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2016.