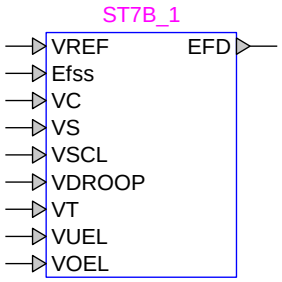
Exciters and Governors: Exciter ST7B



Exciter ST7B

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1 Description

This device is an implementation of the IEEE type ST7B excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 10 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
VSCL	Input	Stator current limiter	pu
VDROOP	Input	Current compensator	pu
VT	Input	Terminal voltage of synchronous machine	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
EFD	Output	Field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_{PA}**: voltage regulator proportional gain
2. **Time constant T_B**: voltage regulator lag time constant
3. **Time constant T_C**: voltage regulator lead time constant
4. **Time constant T_G**: feedback time constant of inner loop field voltage regulator
5. **Time constant T_F**: excitation control system stabilizer time constant
6. **Gain K_L**: minimum excitation limit gain
7. **Gain K_H**: maximum excitation limit gain
8. **Gain K_{IA}**: PI regulator feedback gain
9. **Time constant T_{IA}**: PI regulator feedback time constant
10. **Maximum voltage V_{max}**: Maximum reference voltage
11. **Minimum voltage V_{min}**: Minimum reference voltage
12. **Maximum regulator output V_{Rmax}**: Maximum regulator output
13. **Minimum regulator output V_{Rmin}**: Minimum regulator output
14. Under Excitation Limiter option: see explanations below.
15. Over Excitation Limiter option: see explanations below.

There are two possible selections for the Under Excitation Limiter option:

1. VUEL not available or added to the reference voltage: this option can be selected when the VUEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VUEL connected to the first high value gate (HV gate)
3. VUEL connected to the last high value gate (HV gate)

There are two possible selections for the Over Excitation Limiter option:

1. VOEL not available or added to the reference voltage: this option can be selected when the VOEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VOEL connected to the first low value gate (LV gate)
3. VOEL connected to the last low value gate (LV gate)

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2005.