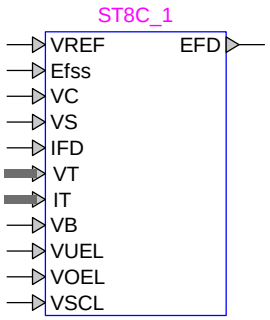
Exciters and Governors: Exciter ST8C



Exciter ST8C

Tshibain Tshibungu, Jean Mahseredjian, 5/8/2017 2:46 PM

1 Description

This device is an implementation of the IEEE type ST8C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 12 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	Input	Field current signal	pu
VT	Input, bundle	Terminal voltage (phasor) of synchronous machine (magnitude and phase)	pu
IT	Input, bundle	Current (phasor) of synchronous machine (magnitude and phase)	pu
VB	Input	Available exciter voltage	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	Field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Gain K_{PR}**: voltage regulator proportional gain
2. **Gain K_{IR}**: voltage regulator integral gain
3. **Maximum regulator output V_{PImax}**: maximum voltage regulator output
4. **Minimum regulator output V_{PImin}**: minimum voltage regulator output
5. **Gain K_{PA}**: field current regulator proportional gain
6. **Gain K_{IA}**: field current regulator integral gain
7. **Maximum field current V_{Amax}**: maximum field current regulator output
8. **Minimum field current V_{Amin}**: minimum field current regulator output
9. **Gain K_A**: field current regulator proportional gain
10. **Time constant T_A**: controlled rectifier bridge equivalent time constant
11. **Maximum field current V_{Rmax}**: maximum field current regulator output
12. **Minimum field current V_{Rmin}**: minimum field current regulator output
13. **Gain K_F**: exciter field current feedback gain
14. **Time constant T_F**: field current feedback time constant
15. **Rectifier loading factor K_{C1}**: rectifier loading factor proportional to commutating reactance
16. **Rectifier loading factor K_{C2}**: rectifier loading factor proportional to commutating reactance
17. **Gain K_P**: potential circuit (voltage) gain coefficient
18. **Phase angle $Theta_P$**: potential circuit phase angle (degrees)
19. **Gain K_{I1}**: potential circuit (current) gain coefficient
20. **Gain K_{I2}**: potential circuit (current) gain coefficient
21. **Reactance X_L**: reactance associated with potential source
22. **Voltage V_{B1max}**: maximum available exciter voltage
23. **Voltage V_{B2max}**: maximum available exciter voltage
24. Excitation Type option: see explanations below.
25. Under Excitation Limiter option: see explanations below.
26. Over Excitation Limiter option: see explanations below.
27. Stator Current Limiter option: see explanations below.

There are two possible selections for the Excitation Type option:

1. Excitation system is self-excited: VT and IT inputs must be connected.
2. Excitation system comes from a separate source: VB input must be connected

There are two possible selections for the Under Excitation Limiter option:

1. VUEL not available or added to the reference voltage: this option can be selected when the VUEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VUEL connected to the high value gate (HV gate)

There are two possible selections for the Over Excitation Limiter option:

1. VOEL not available or added to the reference voltage: this option can be selected when the VOEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VOEL connected to the low value gate (LV gate).

There are three possible selections for the Stator Current Limiter option:

1. VSCL not available or added to the reference voltage: this option can be selected when the VSCL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VSCL connected to the high value gate (HV gate).
3. VSCL connected to the low value gate (LV gate).

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2016.