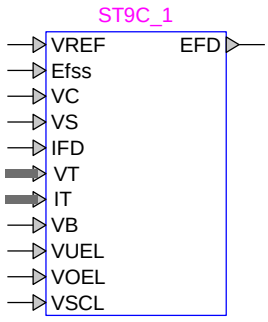
# Exciters and Governors: Exciter ST9C




**Exciter ST9C**



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## 1 Description

This device is an implementation of the IEEE type ST9C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

## 1.1 Pins

This device has 12 pins:

| Pin name | Type | Description | Units |
|---|---|---|---|
| VREF | Input | Reference voltage of the stator terminal voltage | pu |
| Efss | Input | Steady-state field voltage at t = 0, for initialization | pu |
| VC | Input | Terminal voltage of synchronous machine, transducer output | pu |
| VS | Input | Power System Stabilizer signal | pu |
| IFD | Input | Field current signal | pu |
| VT | Input, bundle | Terminal voltage (phasor) of synchronous machine (magnitude and phase) | pu |
| IT | Input, bundle | Current (phasor) of synchronous machine (magnitude and phase) | pu |
| VB | Input | Available exciter voltage | pu |
| VUEL | Input | Under Excitation Limiter signal | pu |
| VOEL | Input | Over Excitation Limiter signal | pu |
| VSCL | Input | Stator Current Limiter signal | pu |
| EFD | Output | Field voltage signal | pu |

## 1.2 Parameters

The default set of parameters can be found in [1].

### 1.2.1 Data tab

The parameters on the Data tab are:

1. **Time constant $T_{CD}$**: time constant of differential part of AVR
2. **Time constant $T_{BD}$**: filter time constant of differential part of AVR
3. **Gain $K_A$**: AVR gain
4. **Gain $K_U$**: gain associated with activation of takeover UEL
5. **Time constant $T_A$**: time constant of AVR
6. **Time constant $T_{AUEL}$**: time constant of underexcitation limiter
7. **Gain $K_{AS}$**: power converter gain (proportional to supply voltage)
8. **Maximum output $V_{Rmax}$**: maximum regulator output
9. **Minimum output $V_{Rmin}$**: minimum regulator output
10. **Rectifier loading factor $K_C$**: rectifier loading factor proportional to commutating reactance
11. **Gain $K_P$**: potential circuit (voltage) gain coefficient
12. **Phase angle $Theta_P$**: potential circuit phase angle (degrees)
13. **Gain $K_I$**: potential circuit (current) gain coefficient
14. **Reactance $X_L$**: reactance associated with potential source
15. **Voltage $V_{Bmax}$**: maximum available exciter voltage
16. Excitation Type option: see explanations below.
17. Under Excitation Limiter option: see explanations below.
18. Over Excitation Limiter option: see explanations below.
19. Stator Current Limiter option: see explanations below.

There are two possible selections for the Excitation Type option:

1. Excitation system is self-excited: VT and IT inputs must be connected.
2. Excitation system comes from a separate source: VB input must be connected

There are two possible selections for the Under Excitation Limiter option:

1. VUEL not available or added to the reference voltage: this option can be selected when the VUEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VUEL connected to the high value gate (HV gate)

There are two possible selections for the Over Excitation Limiter option:

1. VOEL not available or added to the reference voltage: this option can be selected when the VOEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VOEL connected to the low value gate (LV gate).

There are three possible selections for the Stator Current Limiter option:

1. VSCL not available or added to the reference voltage: this option can be selected when the VSCL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VSCL connected to the high value gate (HV gate).
3. VSCL connected to the low value gate (LV gate).

# 2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

# 3 References

[1] “IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies,” IEEE Standard 421.5-2016.