Exciters and Governors: Power System Stabilizer IEEEST

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1 Description

This device is an implementation of the IEEE type IEEEST power system stabilizer model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 2 pins:

Pin name	Type	Description	Units
VSI	Input	PSS input signal. Typical inputs: Synchronous machine speed deviation, acceleration power or electrical power	pu
VSS	Output	PSS output (equivalent of terminal voltage)	pu

1.2 Parameters

The default set of parameters were derived from PSS1A in [2].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Time constant T_5**: time constant
2. **Time constant T_6**: time constant
3. **Gain K_S**: power system stabilizer gain
1. **Filter constant A_1**: PSS signal conditioning frequency filter constant
2. **Filter constant A_2**: PSS signal conditioning frequency filter constant
3. **Filter constant A_3**: PSS signal conditioning frequency filter constant
4. **Filter constant A_4**: PSS signal conditioning frequency filter constant

5. **Filter constant A_5**: PSS signal conditioning frequency filter constant
6. **Filter constant A_6**: PSS signal conditioning frequency filter constant
7. **Lead time constant T_1**: Lead time constant
8. **Lead time constant T_3**: Lead time constant
9. **Lag time constant T_2**: Lag time constant
10. **Lag time constant T_4**: Lag time constant
11. **Maximum output L_{SMAX}**: PSS maximum output signal
12. **Minimum output L_{SMIN}**: PSS minimum output signal

2 Initial conditions

The initial output signal is zero from the steady-state solution.

3 References

[1] "Excitation System Models for Power System Stability Studies," IEEE Committee report. IEEE Transactions on power Apparatus and Systems, Vol.PAS-100. No. 2, Feb. 1981

[2] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2005.