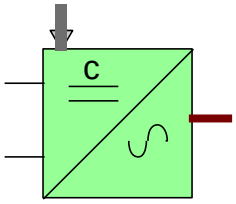
Three-phase Grid-connected Converter

Inverter_3Phase_1



Hossein Ashourian, Henry Gras, 11/25/2022 4:00 PM

1 Description

This document presents a generic EMTP model for three-phase grid-connected converter. It can be used for stability, fault, harmonic, dynamic, and interconnection studies. The converter is a three-phase grid-connected voltage source converter (VSC). Its control system is based on the dq vector current-control approach. Thus, it can naturally limit the current flowing into the converter during disturbances. The basic principle of vector-current control is to regulate the instantaneous active and reactive powers independently through a fast inner current control loop. By using a dq decomposition technique with the grid voltage as phase reference, the inner current control loop decouples the current into d and q components. Outer loops can use the d-component to control converter active power or DC-link voltage, and the q-component to control converter reactive power, converter voltage or converter power factor [1], [2]. The converter has power-frequency and reactive power-voltage droop controls to support grids considering both under and over frequency and voltage events. The converter control system can be either coupled positive-sequence control or decoupled positive- and negative-sequence control.

The converter model can be either Detailed (DM), in which case the IGBT are represented, or Average-Value (AVM), in which case ideal voltage sources follow the voltage reference calculated by the inner-control loops. The DC link of the converter can be connected to either photovoltaic module, battery energy storage or a constant DC voltage source.

A step-up transformer may be included between the converter and Point of Interconnection (POI).

The converter model is aggregated. The converter and the control systems include the necessary nonlinearities, transient and protection functions to simulate accurately the transient behavior of the converter to external power system disturbances. The model is valid for load-flow, time-domain and frequency scan simulation types.

2 Converter Pins and Device Mask

The section describes the converter pins and device mask.

2.1 Converter pins

This device has 4 pins:

Table 1 Converter model Pins

Pin name	Port type	Description	Units
P (+)	Single-phase power	Positive pole of the DC link	
N	Single-phase power	Negative pole of the DC link	
refs	Control input bundle	Pref: Active power, Qref: reactive power Vdcref: DC-link voltage Vacref: AC voltage, and power factor reference inputs in per unit See here how to use bundle.	pu
PCC	3-phase power	Point of Common Coupling	

2.2 Parameters

General tab

- **Number of aggregated inverters:** Number of parallel-connected inverters
- **Frequency:** Grid frequency in Hz
- **Inverter AC voltage:** Voltage on the AC side of the inverter in kVRMSLL
- **Inverter rated power:** Rated apparent power of a single inverter in MVA, kVA, or VA
- **DC voltage:** DC-link voltage in kV
- **DC capacitor:** DC-link capacitor in kJ/MVA
- **Choke resistance:** Choke resistance in pu
- **Choke inductance:** Choke inductance in pu
- **Filter reactive power:** Reactive power generated by each inverter harmonic filter in MVAR, kVAR, or VAR. See 3.4.1 for more information on the filter
- **Number of inverters in service:** Number of parallel-connected inverters in service
- **Outer loop d-axis control mode:** P-control, or VDC-control
- **Outer loop q-axis control mode:** Q-control, VAC control, or PF-control
- **Initial active power:** initial inverter active power reference in pu
- **Initial reactive power:** initial inverter reactive power reference in pu
- **Initial DC-link voltage:** initial inverter DC-link voltage reference in pu
- **Initial AC voltage:** initial inverter AC voltage reference in pu
- **Initial power factor:** initial inverter power factor reference:
- **Initialization (participate in the load-flow solution):** Type of initialization.

  If 'Initialization (participate in the load-flow solution)' is selected, a load-flow bus and an ideal voltage source are added at the point-of-connection of the converter.

  The device participates to the load-flow solution as either a PQ or PV bus. At the beginning of the simulation, the ideal voltage source remains connected to hold the load-flow conditions until the converter is initialized.

  The initialization time is 0.05s. After this time, the ideal voltage source is disconnected.
- **Use control reference variations ($\Delta refs$) for inputs:** If this option is checked, the signals of the *ref* input bundle are control reference variations in pu. At any time, the outer loop control references are the initial references defined above plus these variations.

  If this option is not selected, the signals of the *ref* bundle are the references used by the outer loops. In this case, it is the user responsibility to make sure the initial references in the bundle match the one in the mask, the latter being used for load-flow and initialization, to avoid initialization problems.

Inverter Transformer tab

The 'Nominal three-phase nameplate input' transformer model from the standard EMTP library is used.

In the converter transformer tab, the data must insert for the one converter transformer. The converter model is aggregated. Therefore, the converter transformer is aggregated according to number of aggregated converters, which is automatically done by a script. The total nominal power of one aggregated converter transformer is equal to one converter transformer nominal power multiplied by the number of aggregated converters.

- **Include step-up transformer:** If this option is checked, the converter transformer included and connected between the converter and the grid.
- **Connection Type:** YgYg, DYg, YgD, or DD
- **Nominal power:** Nominal power of a single transformer in MVA
- **Nominal frequency:** Nominal frequency of the transformer in Hz
- **Grid side voltage:** Nominal voltage transformer on the grid side in kVRMSLL
- **Converter side voltage:** Nominal voltage transformer on the converter side in kVRMSLL
- **Winding R:** Winding resistance in pu

- **Winding X:** Winding reactance in pu
- **Winding impedance on winding 1:** Winding impedance on winding 1, distribution ratio
- **Magnetization data:** Current -flux data in pu-pu or A-Wb
- **Magnetization resistance:** Magnetization resistance in pu or Ω
- **Exclude magnetization branch model:** If this option is checked, the magnetization branch model is excluded.

Converter Control tab

- **Converter model:** AVM, average value model or DM, detailed model
- **PWM frequency:** PWM frequency in Hz
- **Type of control:** Coupled control or decoupled-sequence control
- **Sampling rate:** Sampling rate frequency in Hz
- **Cut-off frequency:** Cut-off frequency of measuring input filters in Hz

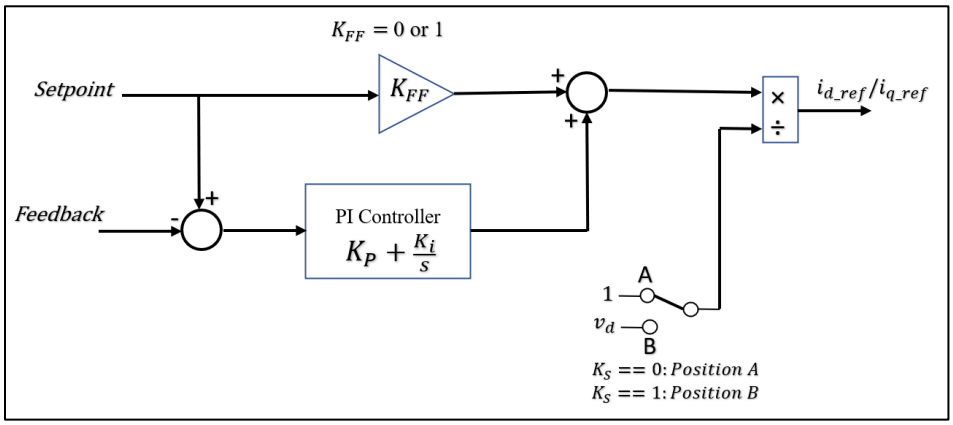


Figure 1 Simplify block diagram of “outer loop dq-axis control”: feedforward and PI controller parameters.

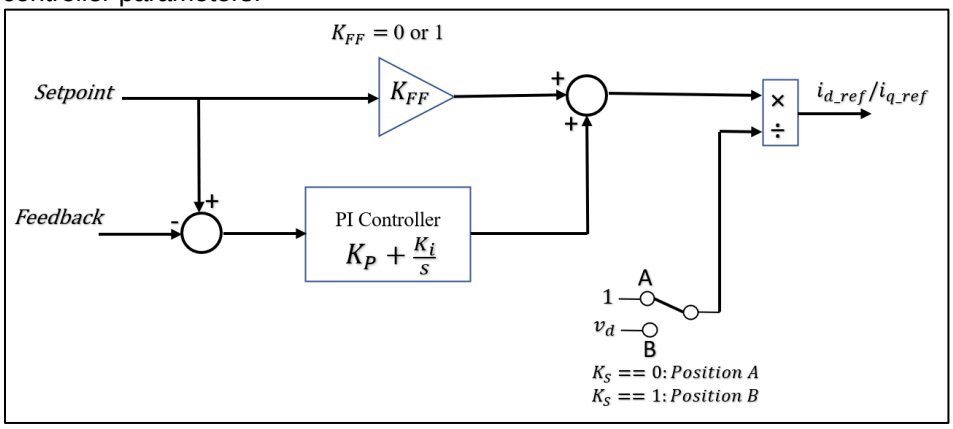


Figure 2 Simplify block diagram of “outer loop dq-axis control”: feedforward and PI controller parameters.

- $\boldsymbol{K_{FF}}$**:** Feedforward gain. It must be 0 or 1. When it set to 0, the feedforward path is excluded.
- $\boldsymbol{K_S}$**:** d-axis voltage gain. It must be 0 or 1. When it set to 1, the output reference signal is divided by Vd. When it set to 0, the output reference signal is divided by 1.
- **PI control dynamic parameters:** Time constant or PI regulator gains
- **d-axis control time constant:** d-axis outer closed-loop control Time constant in s
- **q-axis control time constant:** q-axis outer closed-loop control Time constant in s
- **d-axis control** $\boldsymbol{K_i}$**:** d-axis outer loop control PI controller, integral gain
- **d-axis control** $\boldsymbol{K_p}$**:** d-axis outer loop control PI controller, proportional gain

- **q-axis control K_i:** q-axis outer loop control PI controller, integral gain
- **q-axis control K_p:** q-axis outer loop control PI controller, proportional gain

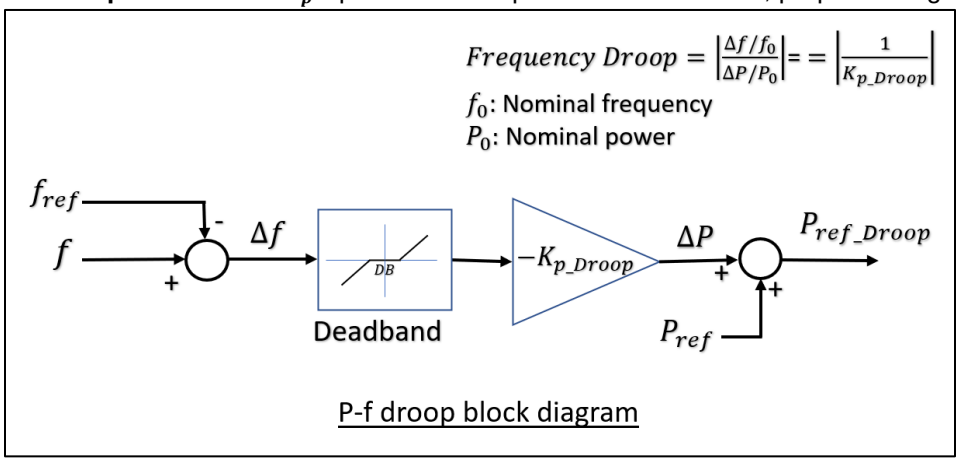


Figure 3 P-f and Q-V droop control block diagrams

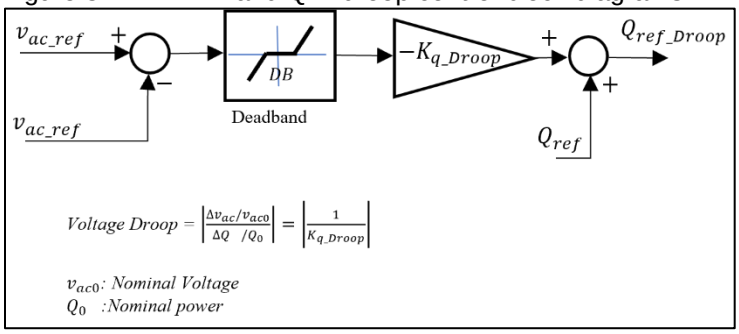


Figure 4 Q-V droop control block diagram, closed-loop reactive power control

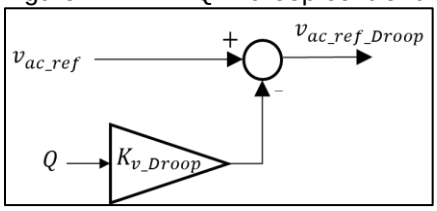


Figure 5 Q-V droop control block diagram, closed-loop ac voltage control

- **$K_{p-Droop}$:** Droop coefficient of P-f droop control in pu
- **Frequency Deadband:** Frequency deadband of P-f droop control in pu
- **$K_{q-Droop}$:** Droop coefficient of Q-V droop control, closed-loop reactive power control in pu
- **Voltage Deadband:** Voltage deadband of Q-V droop control in pu
- **$K_{v-Droop}$:** Droop coefficient of Q-V droop control, closed-loop voltage control in pu
- **R_{sys}:** Equivalent resistance of the external network in Ω
- **X_{sys}:** Equivalent reactance of the external network in Ω
- **Rise time:** Closed-loop current control rise-time in ms
- **Current limit:** Converter current limit in pu
- **d-axis current limit:** Converter d-axis current limit in pu
- **q-axis current limit:** Converter q-axis current limit in pu
- **PLL K_i:** PLL PI controller, integral gain
- **PLL K_p:** PLL PI controller, proportional gain
- **FRT q-axis current injection gain:** q-axis current injection gain during FRT in pu
- **FRT_ON:** Minimum FRT voltage deviation, FRT function is activated when voltage deviation from 1 pu (dV) is larger than FRT_ON in pu

- **FRT_OFF:** FRT reset voltage deviation, FRT function is deactivated when (dV < FRT_OFF) & (t_FRT > FRT_time) in pu
- **FRT_time:** FRT reset delay, FRT function is deactivated when (dV < FRT_OFF) & (t_FRT > FRT_time) in s
- **FRT current limit:** Current limit during FRT in pu
- **FRT q-axis current limit:** q-axis current limit during FRT in pu

Protection tab

- **Enable voltage sag protection:** If this option is checked, the voltage sag protection is enabled.
- **Pickup DVS voltage:** Threshold voltage value to activate the Deep-Voltage-Sag (DVS) protection in pu
- **Reset DVS voltage:** Threshold voltage value to deactivate the Deep-Voltage-Sag protection in pu
- **Enable chopper protection:** If this option is checked, the chopper protection is enabled.
- **Pickup Vdc:** Chopper ON when Vdc is above this value in pu
- **Reset Vdc:** Chopper OFF when Vdc below this value in pu
- **Enable overcurrent protection:** If this option is checked, the overcurrent protection is enabled.
- **Converter pickup current:** Converter overcurrent protection threshold in pu
- **Reset delay:** Overcurrent protection release delay in s
- **Enable AC undervoltage protection:** If this option is checked, the AC undervoltage protection is enabled.
- **AC undervoltage protection data:** Voltage versus time curve for the AC under voltage protection in s and pu
- **Enable AC overvoltage protection:** If this option is checked, the AC overvoltage protection is enabled
- **AC overvoltage protection data:** Voltage versus time curve for the AC under voltage protection in s and pu

Harmonics tab

- **Use harmonic model for steady-state and time-domain simulations:** If this option is checked, this device is modeled as a harmonic current source for Steady-state and Time-domain simulations.
- **Use harmonic model for frequency-scan simulations:** If this option is checked, the Fundamental frequency current magnitude input and the first line of the Harmonic data table are adjusted to match the Load-Flow solution current.
-
- **Adjust fundamental frequency current to match Load-Flow solution results:** If this option is checked, this device is modeled as a harmonic current source during Frequency scan simulations
- **Fundamental frequency current magnitude (for one inverter)**: Magnitude of the fundamental frequency current for 1 inverter in A RMS. This value is automatically multiplied by the number of inverters in service.
- **Harmonics data table:** Harmonic contents [harmonic number, I mag(%), I Angle (deg), Z(Ohm), Z Angle(deg)] for phase A (balanced source)

3 Converter device model

3.1 General

The general structure of the converter model is shown in Figure 6.

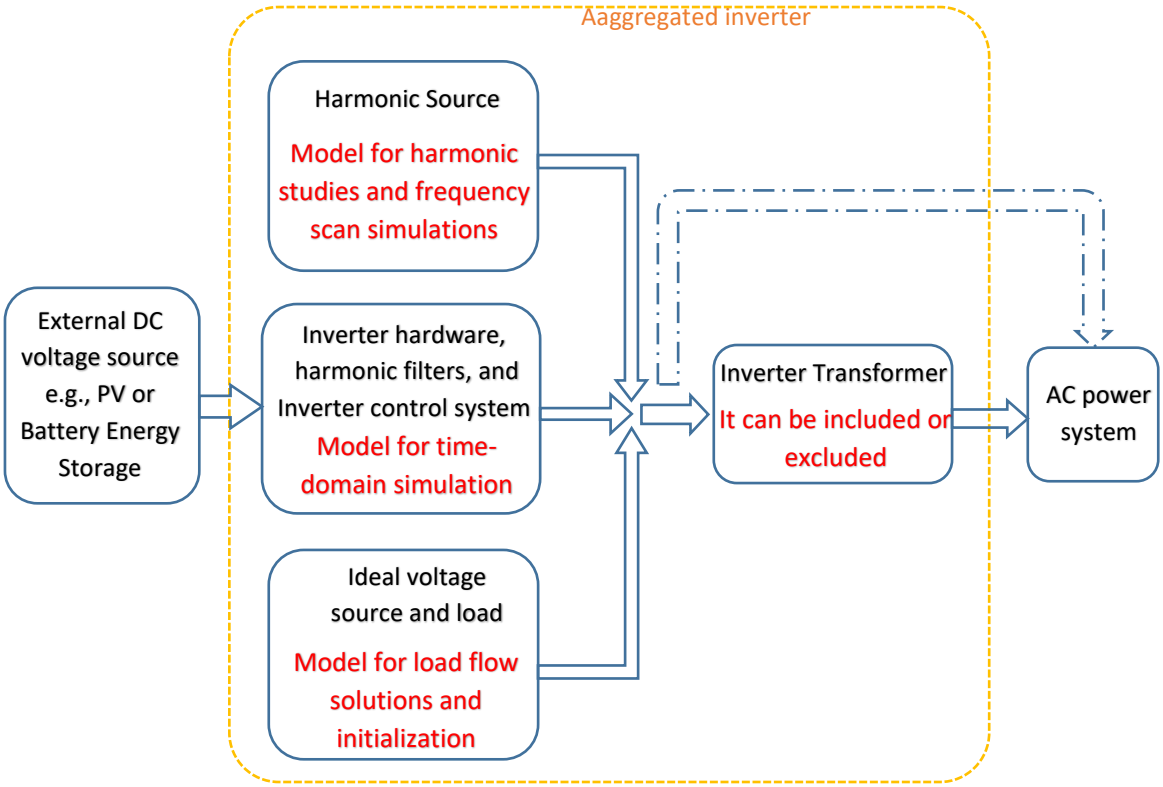


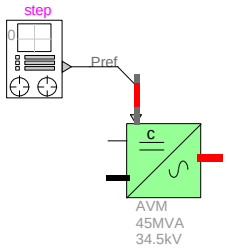
Figure 6 General structure of three-phase grid-following converter model

The converter content is automatically modified according to the simulation type, so the model is valid for any simulation options EMTP offers.

During load-flow, the converter is modelled by a PQ load-flow bus. The load-flow power is the *Initial active power* input, the reactive power is the *Initial reactive power input*.

In time-domain, the model is initialized with the load-flow conditions and the outer loop control initial references are the ones used during load-flow, which were detailed in the section hereabove. The initialization time is t_init =0.05s. During this time, an ideal voltage source is connected to the converter 3-phase pin. This voltage source holds the load-flow conditions while the converter controls are initializing. After this time, the ideal voltage source is disconnected by a switch.

Control power and voltage references may be dynamically varied by changing 2 reference inputs (Pref/Vdcref and Qref/Vacref/PFref) inside the “refs” bundle of the device. See here how to use bundle.



These inputs may either be:

- deviations from the initial references, in which case, they may be set to 0 to maintain load-flow condition in time-domain. The *Use power reference changes for input* option may be checked to enable this option.

- references, in which case, the actual reference value of the outer control loops may be set as inputs.

If an input is set to zero or is not connected, it is assumed to be 0.
The inputs are in per unit and are considered only when they are used by the control selected. For example, Vdcref is considered only if the d-axis outer loop control is Vdc-control and it is not considered if the d-axis outer loop control is P-control.

During frequency-scan analysis, the converter is a Norton harmonic source. It is connected to the low-voltage side of the converter transformer if the latter is included. No control is included when the harmonic representation is selected.

3.2 Converter Modeling

Figure 7 shows the inverter model connected to a 34.5kV equivalent network.

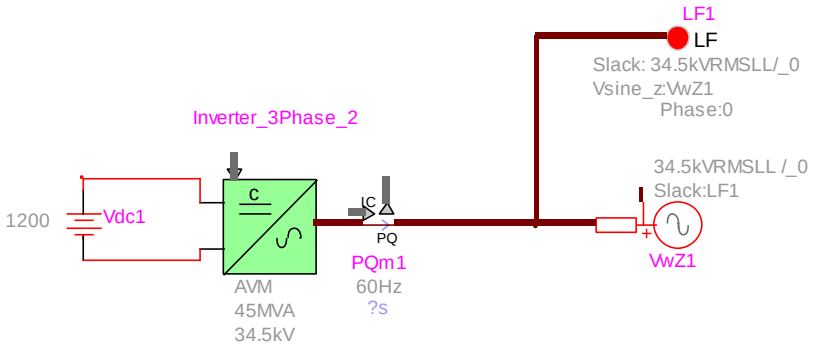


Figure 7 Inverter model connected to a 34.5kV equivalent network

As shown in Figure 8, the inverter model is composed of

- “Inverter hardware” block
- “Inverter Control System” block,
- Inverter transformer (or converter transformer),
- PQ initialization block
- Harmonics block which is a Norton harmonic source for harmonic analysis.

The PQ initialization source contains a load flow device and an ideal voltage source. It prevents large transients at external network and provides flat starting during initialization of inverter electrical and control systems.

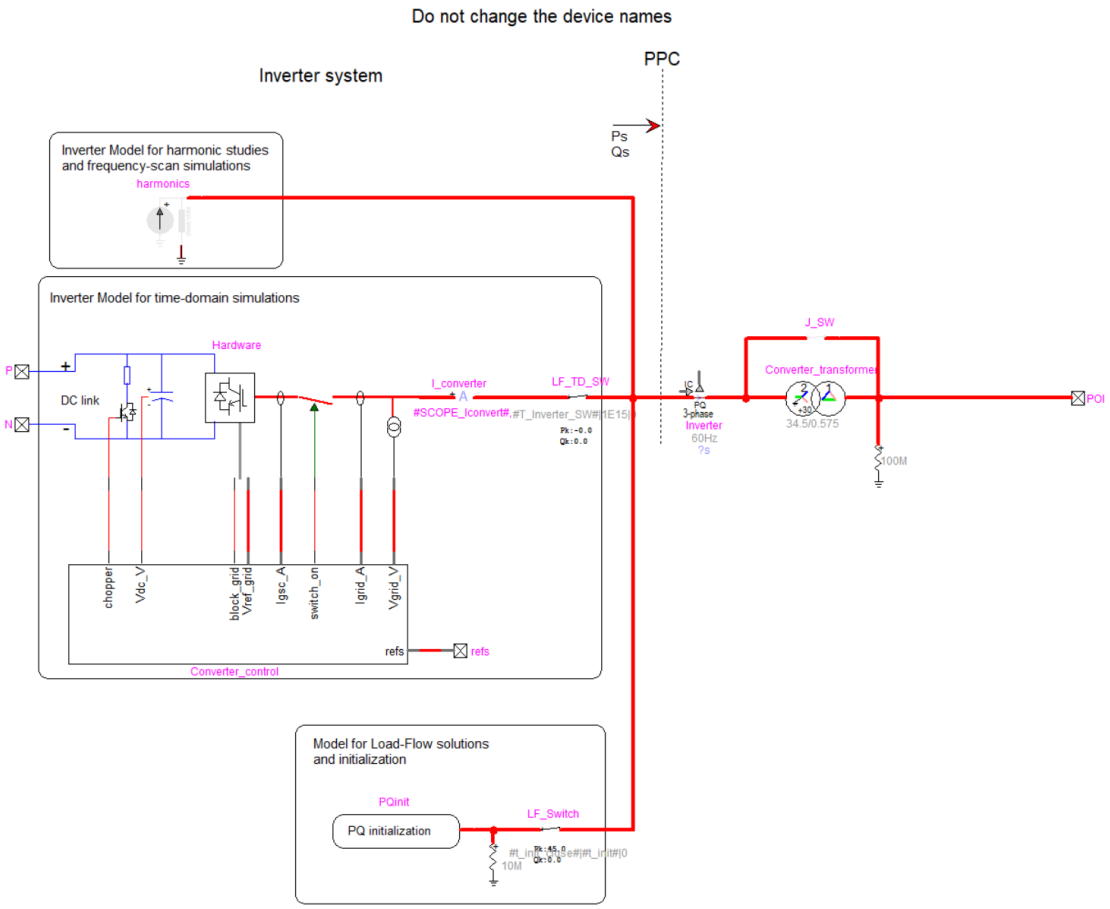


Figure 8 EMTP diagram of the Inverter model

3.3 Hardware

Figure 9 shows the inverter hardware in EMTP. The inverter hardware is composed of a DC-AC converter, a series RL branch (choke filter), two shunt ac harmonic filters, and the current and voltage measurement units used for monitoring and control purposes. All variables are monitored as instantaneous values and meter locations are shown in Figure 9. The DC-AC converter model can be detailed model or average value model. The DC resistive chopper limits the DC bus voltage and is controlled by the protection system block. This option uses when the DC bus is connected to PV or battery systems.

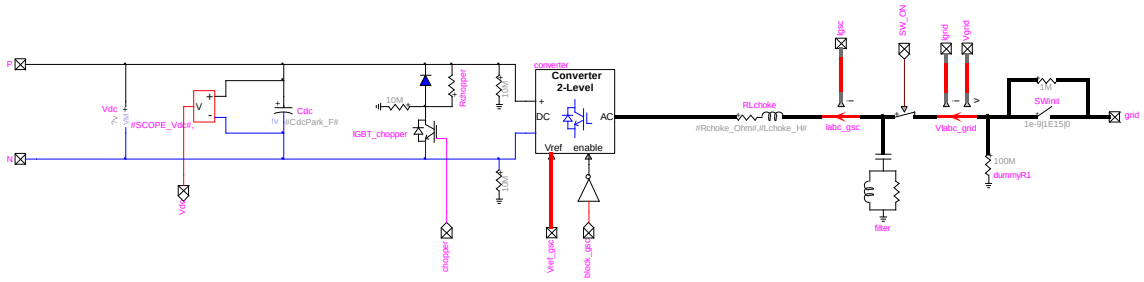


Figure 9 Inverter hardware

3.4 DC-AC converter model: detailed model (DM) and average value model (AVM)

The EMTP diagram of the detailed model (DM) is shown in Figure 10. It includes a two-level voltage source converter (VSC) block and a pulse width modulation (PWM) block.

A detailed two-level topology (Figure 11.a) is used for the VSC in which the valve is composed by one IGBT switch, two non-ideal (series and anti-parallel) diodes and a snubber circuit as shown in Figure 11.b. The non-ideal diodes are modeled as non-linear resistances.

The PWM block receives the three-phase reference voltages from converter control and generates the pulse pattern for the six IGBT switches by comparing the voltage reference with a triangular carrier wave. In a two-level converter, if the reference voltage is higher than the carrier wave then the phase terminal is connected to the positive DC terminal, and if it is lower, the phase terminal is connected to the negative DC terminal. The EMTP diagram of the PWM block is presented in Figure 12.

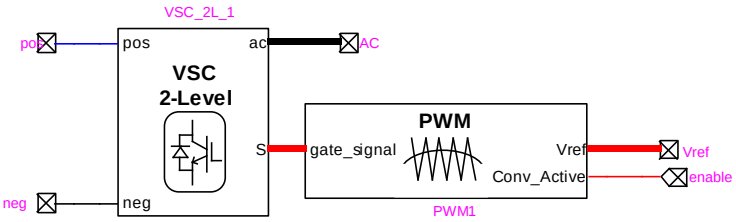


Figure 10 DC-AC converter block inside the inverter hardware model (detailed model version)

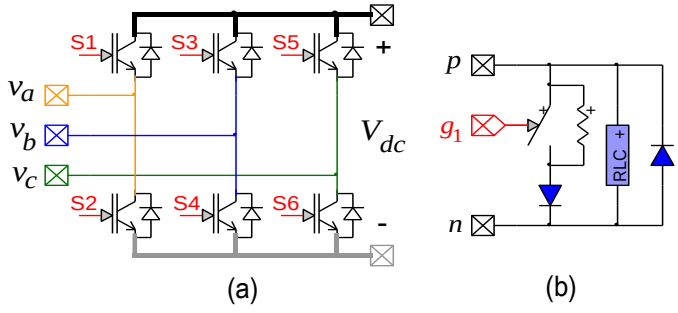


Figure 11 (a) Two-level Converter, (b) IGBT valve

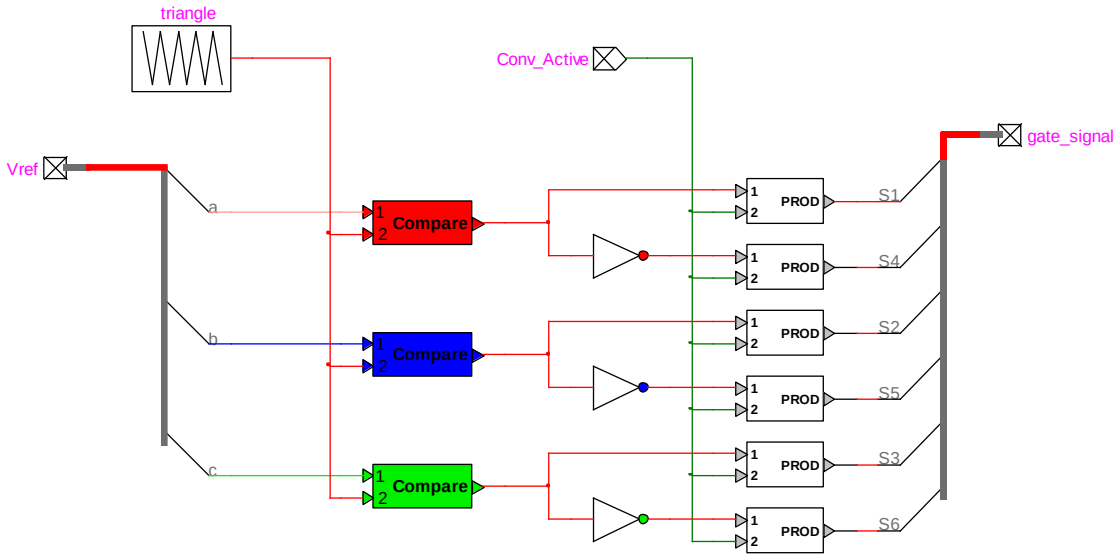


Figure 12 PWM control block

The DM mimics the converter behavior accurately. However, simulation of such switching circuits with variable topology requires many time-consuming mathematical operations and the high frequency PWM signals force small simulation time step usage. These computational inefficiencies can be eliminated by using average value model (AVM) which replicates the average response of switching devices, converters and controls through simplified functions and controlled sources [3] AVMs have been successfully developed for inverter-based technologies [4]. AVM obtained by replacing DM of converters with voltage-controlled sources on the AC side and current-controlled sources on the DC side as shown in Figure 13.

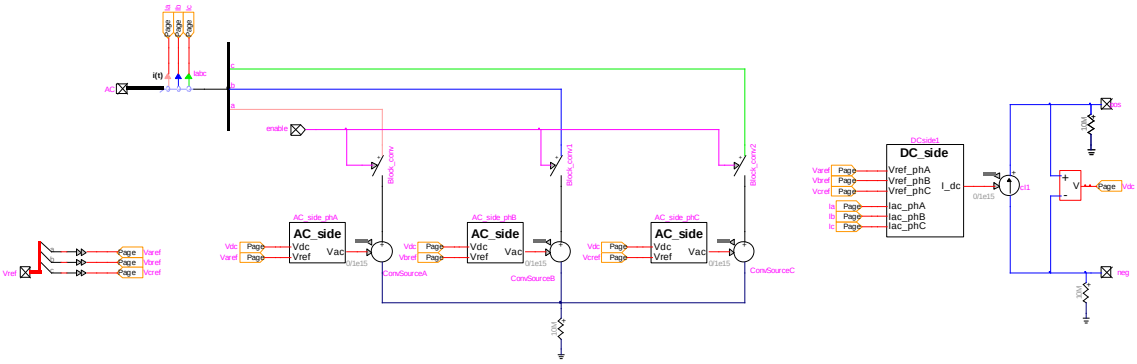


Figure 13 AVM Representation of the VSC

3.4.1 Shunt AC harmonic filters

The “shunt AC harmonic filters” block includes two harmonic filters as shown in Figure 14. These filters are tuned at switching frequencies harmonics n1 and n2. The filter parameters are computed as

$$C_{f1} = \frac{Q_{filter}\ N_{Inv}}{U^2(2\pi f)} \quad (1)$$

$$L_{f1} = \frac{N_{Inv}}{C_{f1}(2\pi f n_1)^2} \quad (2)$$

$$R_{f1} = \frac{(2\pi f)n_1\ L_{f1}\ Q}{N_{Inv}} \quad (3)$$

$$C_{f2} = C_{f1} \quad (4)$$

$$L_{f2} = \frac{N_{Inv}}{C_{f2}(2\pi f n_2)^2} \quad (5)$$

$$R_{f2} = \frac{(2\pi f)n_2\ L_{f2}\ Q}{N_{Inv}} \quad (6)$$

where U is the rated LV grid voltage, Q_{filter} is the reactive power of the filter for one inverter, Q is the quality factor, and N_{Inv} is the number of the parallel inverters. Q_{filter} is set from the inverter mask as shown in **Error! Reference source not found.**. The switching frequencies harmonics n1 and n2 are as follows

$$n_1 = \frac{f_{PWM}}{f_s} \quad (7)$$

$$n_2 = 2n_1 \quad (8)$$

where f_{PWM} is the PWM frequency and f_s is the nominal frequency.

In case another type of filter (LC or LCL filter) or other parameters should be used, the filter can be modified by the user inside the inverter subcircuit. If several inverters are found in the network, the filter subcircuit and its parents must be made unique to avoid modifying all inverters instances.

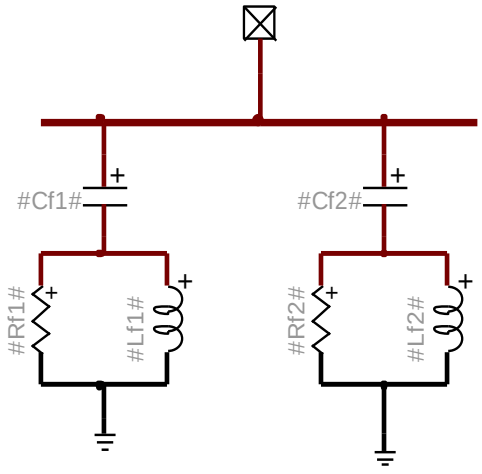


Figure 14 “shunt ac harmonic filter” block

3.5 Inverter control system

The EMTP diagram of the inverter control system block (or “Converter_control” block) is shown in Figure 15. The sampled signals are converted to pu and filtered. The sampling frequency are set to 12.5 kHz and can be modified by the user from the device mask. The “sampling” blocks are deactivated in AVM due to large simulation time step usage. In generic model, 2nd order Bessel type low pass filters are used. The cut-off frequencies of the filters are set to 2.5 kHz and can be modified by the user from the inverter device mask. The order (up to 8th order), the type (Bessel and Butterworth) and the cut-off frequencies of the low pass filters can be modified from device mask. The protection block includes the AC over/under voltage protections, deep voltage sag detector, the DC chopper control, and overcurrent detector. The control system offers both coupled and decoupled sequence control options. User can select the control system options from the device mask as described in 2.

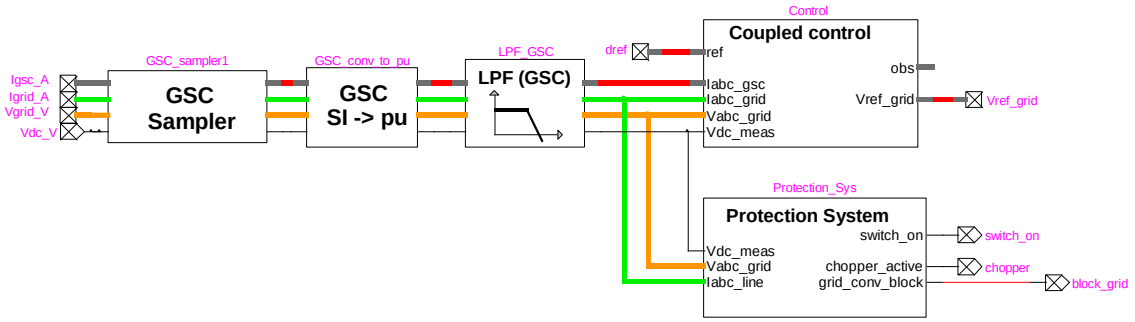


Figure 15 EMTP diagram of the PV inverter control block

3.5.1 Inverter coupled control

The EMTP diagram of the “Coupled Control” block is shown in Figure 16. The “GSC Computing Variables” block does the dq transformation required for the vector control. In “computing variable” block, a synchronous reference frame (SRF) PLL is used to drive the phase angle θ of the rotating reference frame from the inverter terminal voltages, allowing the synchronization of the control parameters with the system voltage [5], [6]. The EMTP diagram of the SRF PLL is shown in Figure 17. Moreover, two abc-to-dq frame transformations are used to transfer voltage and current sinusoidal waveforms to DC quantities (d and q reference frame) waveforms. The transformation matrix T in (9) transforms abc-frame waveforms into dq-frame components rotating at synchronous speed $\omega = d\theta/dt$. In matrix T, the direct axis d is aligned with the grid voltage. If the PLL is in a steady-state condition, the q axis of the inverter voltage terminal is equal to zero [6].

$$\begin{bmatrix} d \\ q \end{bmatrix} = T \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

$$T = \frac{2}{3}\begin{bmatrix} cos(\omega t) & cos(\omega t - 2\pi/3) & cos(\omega t + 2\pi/3t) \\ -sin(\omega t) & -sin(\omega t - 2\pi/3) & -sin(\omega t + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \quad (9)$$

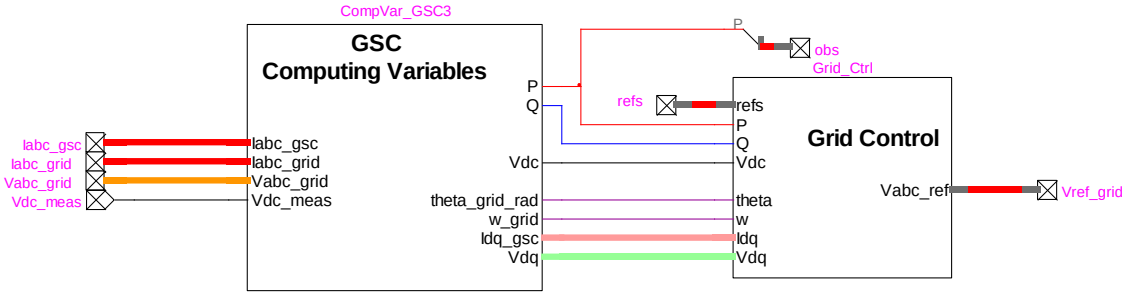


Figure 16 EMTP diagram of “coupled control” block

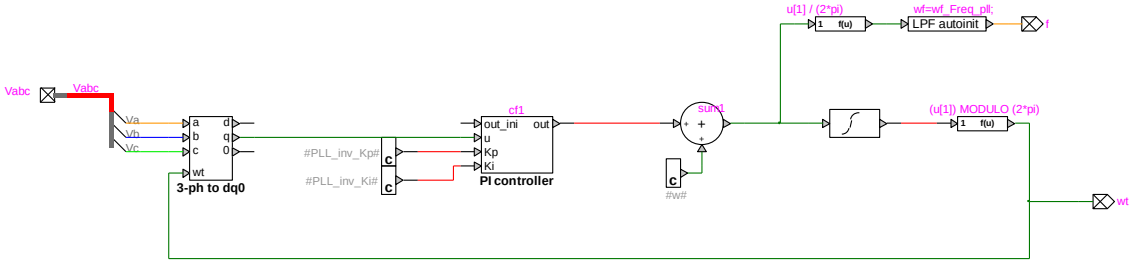


Figure 17 EMTP diagram of SRF PLL

Figure 18 shows EMTP diagram of the “Grid Control” block. It is a current-controlled active and reactive controller in dq-frame. The active and reactive power of inverter are controlled by the line current components i_d and i_q [2], [7],. The reference current commands i_{dref} and i_{qref} for the inner current loop are generated by outer loop control blocks. In the inner current control and linearization blocks, the feedback and feed-forward signals in dq-frame are processed by compensators to make the control signals. Then, they are transformed to the abc-frame and sent to the converter.

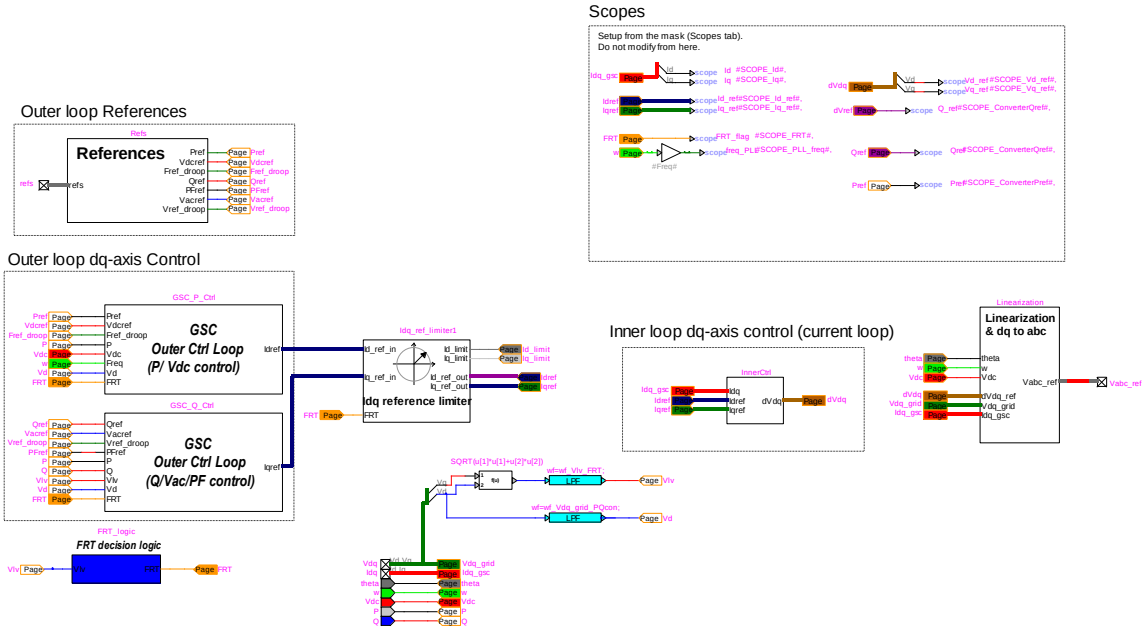


Figure 18 EMTP diagram of “control” block inside the “coupled control” block

3.5.1.1 Inner loop control

The schematic of the inverter connected to the power system through a series RL branch (choke filter) is shown in Figure 19. The dynamic of the AC side of the inverter is given by following equation (bold characters are used for vectors and matrices).

$$\boldsymbol{V}_{abc} = +\boldsymbol{R}\boldsymbol{i}_{gabc} + \boldsymbol{L}\left(\frac{d\boldsymbol{i}_{gabc}}{dt}\right) + \boldsymbol{V}_{gabc} \tag{10}$$

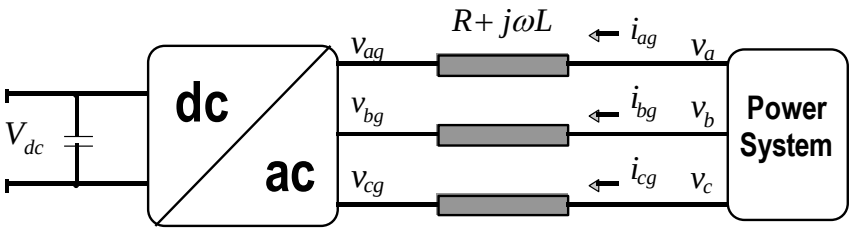


Figure 19 converter arrangement

Applying abc-dq transformation on (10) and using [8], the converter reference voltages are given as follows.

$$v_{dg}^{'} = -\left(k_p + \frac{k_i}{s}\right)\left(i_{dg}^{'} - i_{dg}\right) + \omega L_{choke} i_{qg} + v_{d-choke} \tag{11}$$

$$v_{qg}^{'} = -\left(k_p + \frac{k_i}{s}\right)\left(i_{qg}^{'} - i_{qg}\right) - \omega L_{choke} i_{dg} + v_{q-choke} \tag{12}$$

where K_p and K_i are proportional and integral gains. $(\omega L_{choke} i_{qg} + v_{d-choke})$ and $\left(-\omega L_{choke} i_{dg} + v_{q-choke}\right)$ are feed-forward compensating terms which are added to the d- and q-axis voltages calculated by the PI regulators. $i_{dg}^{'}$ and $i_{qg}^{'}$ (equivalent to i_{dref} and i_{qref} in Figure 18) are reference inverter currents in dq-frame.

During normal operation, the controller gives the priority to the active currents, i.e.

$$\begin{aligned} i_{dg}^{'} &< I_{dg}^{lim} \\ i_{qg}^{'} &< I_{qg}^{lim} = \sqrt{(I_g^{lim})^2 - (i_{dg}^{'})^2} \end{aligned} \tag{13}$$

where I_{dg}^{lim}, I_{qg}^{lim} and I_g^{lim} are the limits for d-axis, q-axis and total converter currents, respectively.

3.5.1.2 Outer loop control

The inverter reference currents $i_{dg}^{'}$ and $i_{qg}^{'}$ (equivalent to i_{dref} and i_{qref} in Figure 18) are generated by the outer loop dq-axis control blocks.

The outer loop d-axis control block is shown Figure 20. It can regulate either inverter active power or DC-link voltage. An active power-frequency (P-f) droop control is added to the active power control loop (see Figure 3 for more details).

The outer loop q-axis control block is shown Figure 21. It can regulate either inverter reactive power, inverter power factor, or inverter AC voltage. A reactive power-voltage (Q-V) droop control is added to the reactive power and voltage control loop (see Figure 4 and Figure 5 for more details).

Depending on setting parameters as shown in Figure 2, the inverter reference currents can be generated using a combination of proportional-integral (PI) controllers according to the difference between measured and desired inverter references. To use the feedforward control, KFF gain must be set to 1 and PI controller gains (KI and Kp) must be set to 0.

Regarding active and reactive power control using the feedforward method, the active and reactive power delivered to the AC power system are calculated as follow [2].

$$P_{inv} = -[V_d i_{dg} + V_q i_{qg}] \quad (14)$$

$$Q_{inv} = -[-V_d i_{qg} + V_q i_{dg}] \quad (15)$$

where V_d and V_q are the AC power system voltage in dq-frame. If the PLL is in steady state, $V_q = 0$. Thus, providing the control system response is fast enough, P_{inv} and Q_{inv} can be controlled by i_{dg} and i_{qg} and reference currents are calculated as follow.

$$i_{dg}^{'}(or\ i_{dref}) = -P_{inv\_ref}/V_d \quad (16)$$

$$i_{qg}^{'}(or\ i_{qref}) = Q_{inv\_ref}/V_d \quad (17)$$

Where P_{inv_ref} and Q_{inv_ref} inverter reference active and reactive powers.

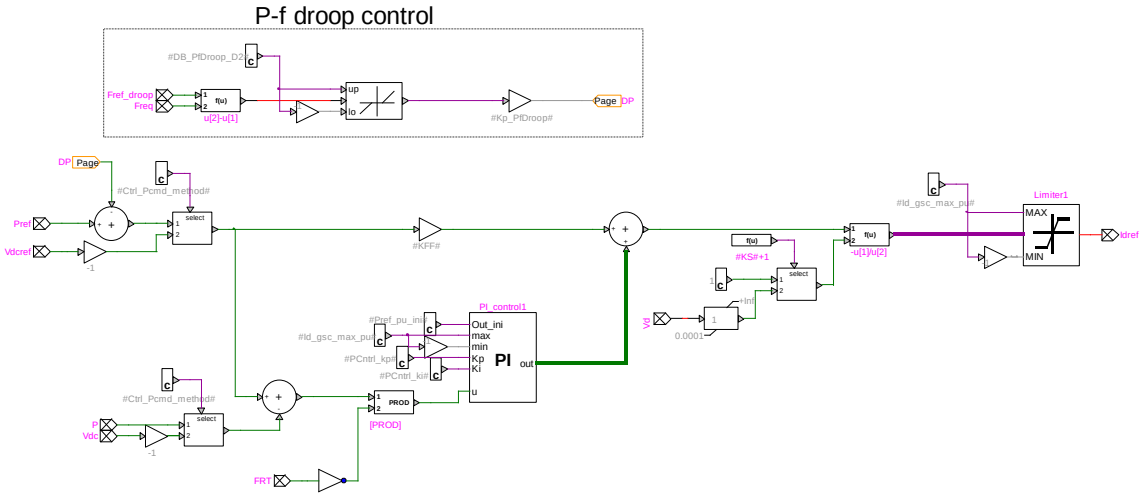


Figure 20 Active power outer control loop

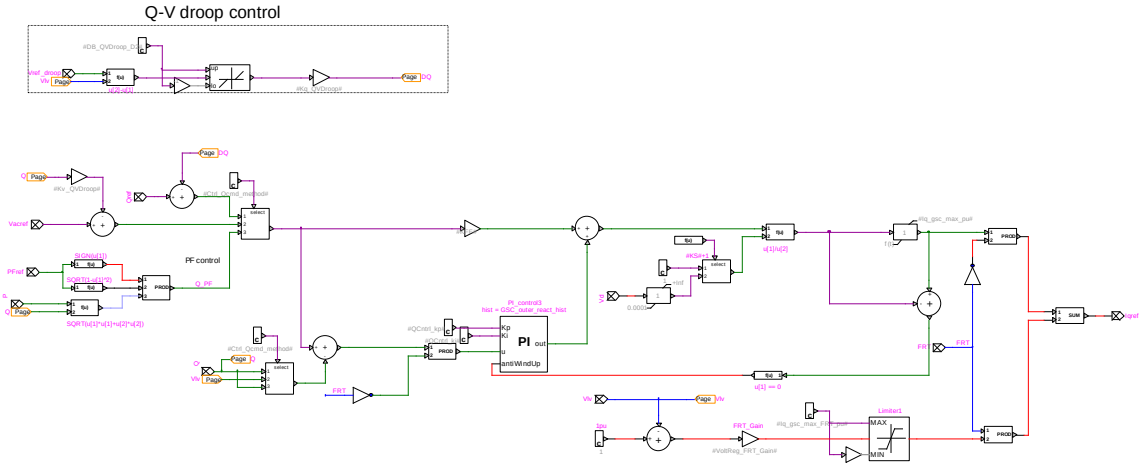


Figure 21 Reactive power outer control loop

3.5.1.3 Fault ride-through (FRT)

The inverter model is equipped with an FRT function to fulfill the grid code requirement regarding voltage support shown in Figure 22. The FRT function is activated when

$$|1 - V_{lv}^{+}| > V_{FRT-ON} \tag{18}$$

and deactivated when

$$|1 - V_{lv}^{+}| < V_{FRT-OFF} \tag{19}$$

after a pre-specified release time t_{FRT}. V_{lv}^{+} is inverter voltage terminal amplitude
When FRT function is active, the inverter controller gives the priority to the reactive current by reversing the d- and q-axis current limits given in (15), i.e.

$$\begin{aligned} i_{qg}^{'} &< I_{qg}^{lim} \\ i_{dg}^{'} &< I_{dg}^{lim} = \sqrt{(I_{g}^{lim})^2 - (i_{qg}^{'})^2} \end{aligned} \tag{20}$$

The EMTP diagram of “Idq reference limiter” and “FRT decision logic” blocks are given in Figure 23 and Figure 24, respectively. The limits for d-axis, q-axis and total inverter currents and FRT function thresholds can be modified from the device mask as shown in 2.

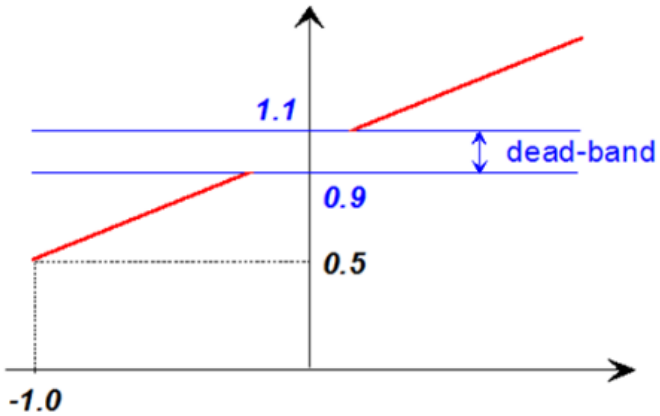


Figure 22 Inverter reactive output current during voltage disturbances [9]

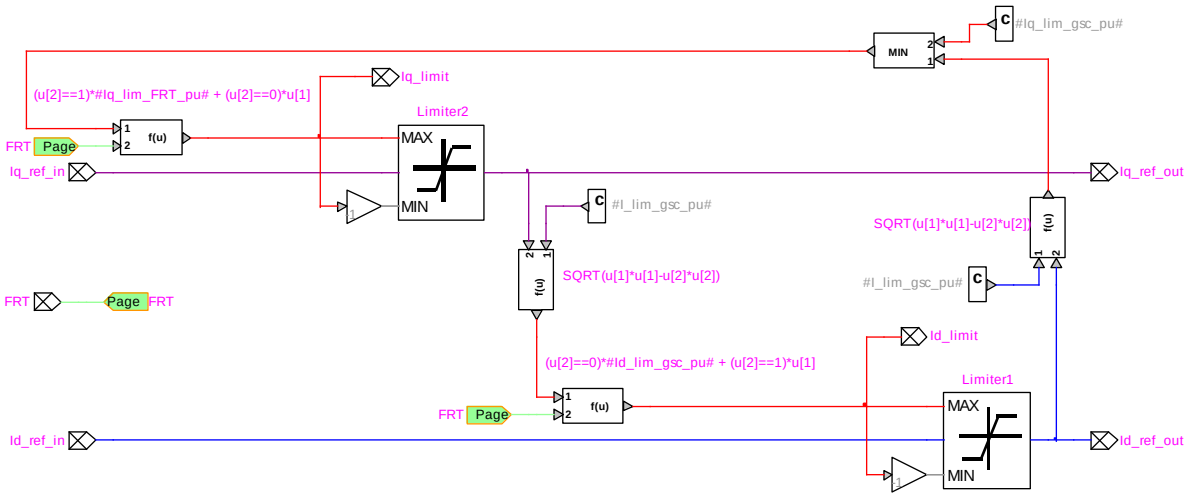


Figure 23 EMTP diagram of "I_{dq} reference limiter" block

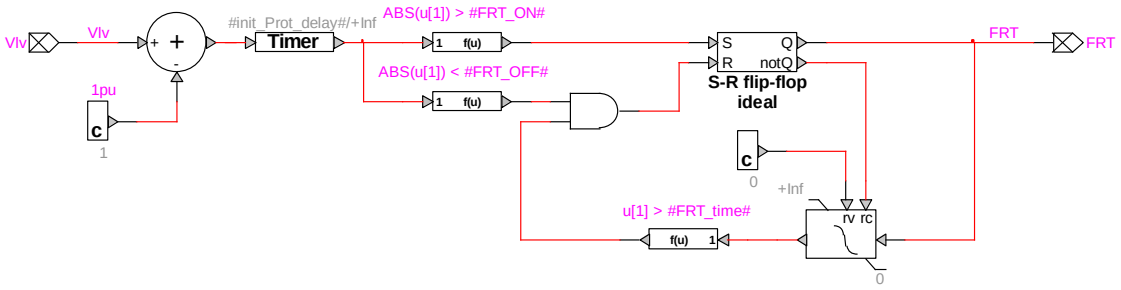


Figure 24 EMTP diagram of "FRT decision logic" block

3.5.2 Inverter decoupled sequence control

The EMTP diagram of the Decoupled Control" block is shown in Figure 25 . The phase angle θ of the rotating reference frame is derived by the double synchronous reference frame (DSRF) PLL in the decoupled control [10] from the inverter terminal voltages. It allows the synchronization of the control parameters with the system voltage. Figure 26 shows EMTP diagram of DSRF PLL. Figure 27 show the EMTP diagram of the Grid control block.

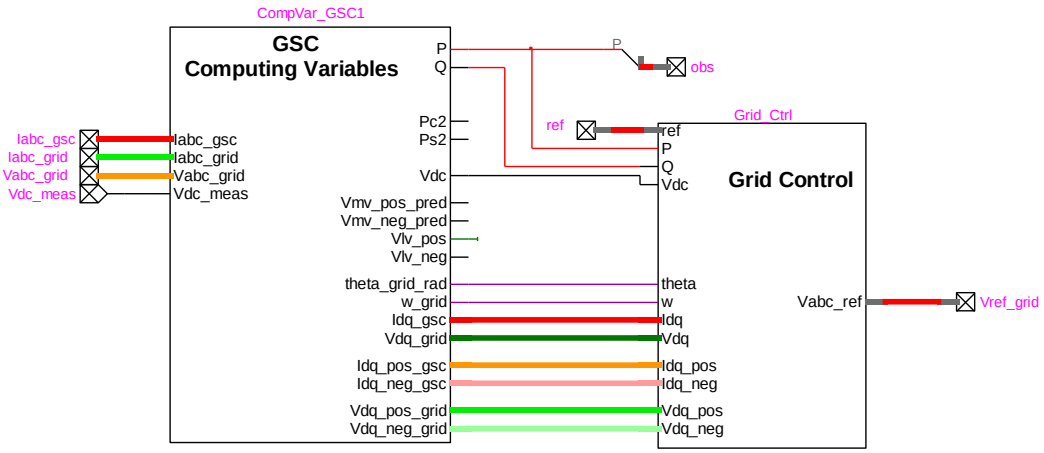


Figure 25 EMTP diagram of Decoupled Control block

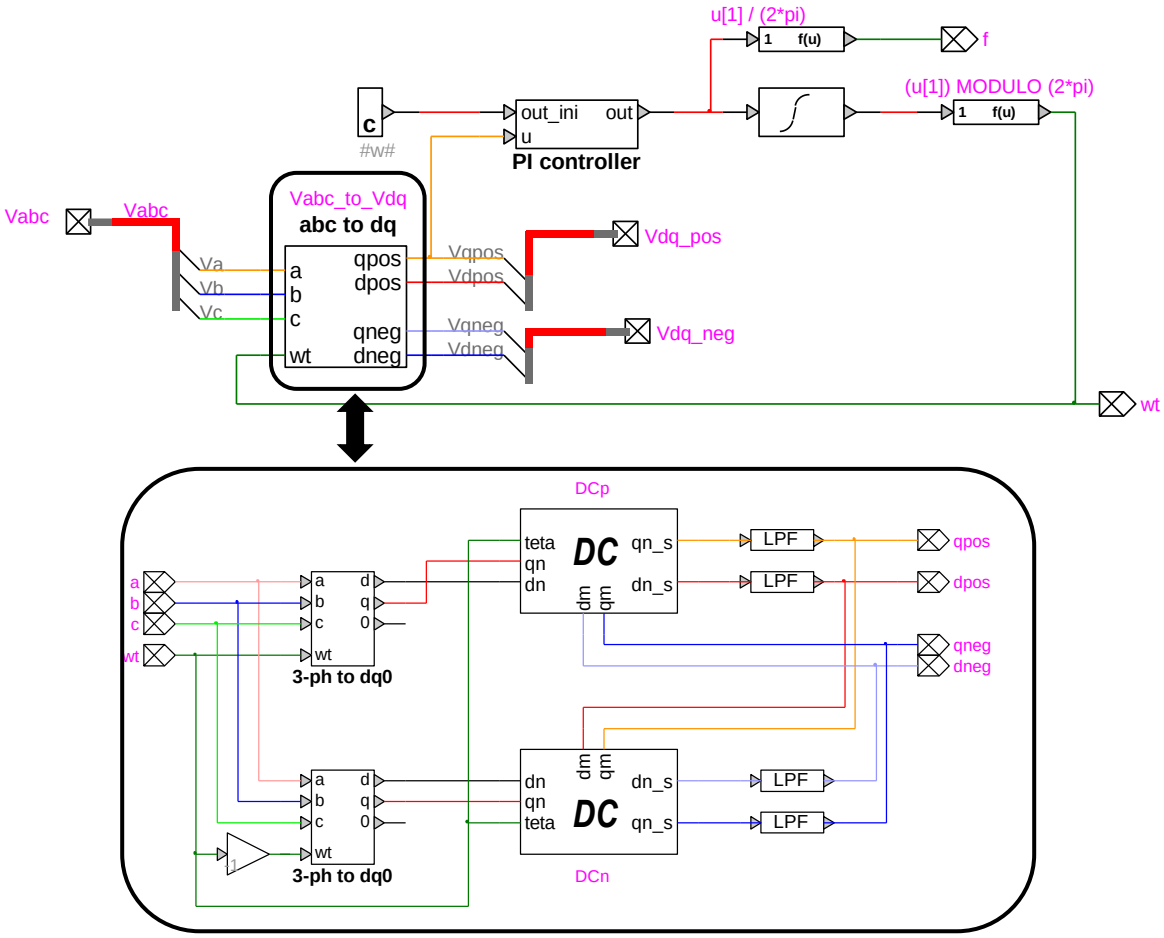


Figure 26 EMTP diagram of DSRF PLL

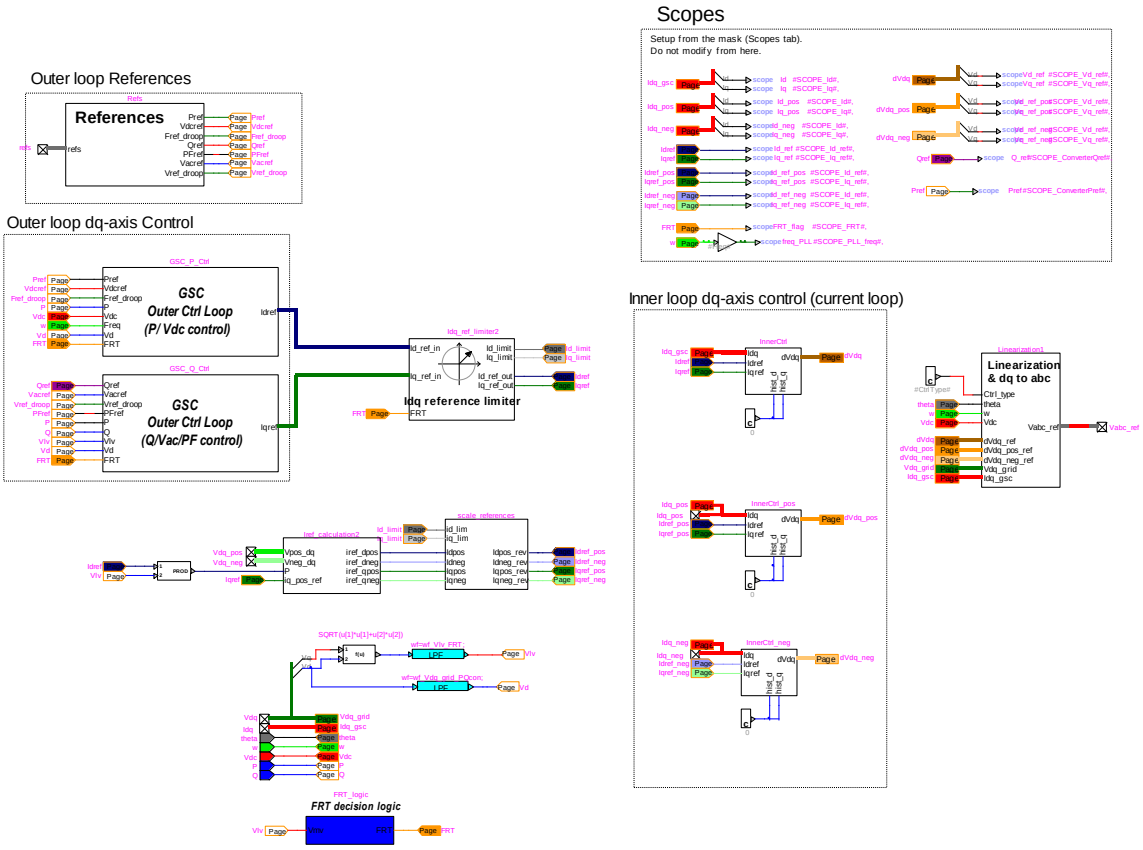


Figure 27 EMTP diagram of “control” block inside the “decoupled control” block

Ideally, the inverter control presented in the previous section is not expected to inject any negative sequence currents to the grid during unbalanced loading conditions or faults. However, the terminal voltage of inverter contains negative sequence components during unbalanced loading conditions or faults. This causes second harmonic power oscillations in inverter power output. The instantaneous active and reactive powers such unbalanced grid conditions can be also written as [11]

$$p = P_0 + P_{C2}\,cos(2\omega t) + P_{S2}\,cos(2\omega t) \qquad (21)$$

$$q = Q_0 + Q_{C2}\,cos(2\omega t) + Q_{S2}\,cos(2\omega t) \qquad (22)$$

where P_0 and Q_0 are the average values of the instantaneous active and reactive powers respectively, whereas P_{C2}, P_{S2}, Q_{C2} and Q_{S2} represent the magnitude of the second harmonic oscillating terms in these instantaneous powers.

With decoupled sequence control usage, four of the six power magnitudes in (21) can be controlled for a given grid voltage conditions. As the oscillating terms in active power P_{C2}, P_{S2} cause oscillations in DC bus voltage V_{dc}, the inverter current references ($i_{dg}^{+\prime}$,$i_{qg}^{+\prime}$,$i_{dg}^{-\prime}$,$i_{qg}^{-\prime}$) are calculated to cancel out these terms (i.e. $P_{C2} = P_{S2} = 0$).

The outer control and Idq limiter shown in Figure 27 calculates $i_{dg}^{'}$, $i_{qg}^{'}$, I_{dg}^{lim} and I_{qg}^{lim}. These values are used to calculate the inverter current references $i_{dg}^{+\prime}$, $i_{qg}^{+\prime}$, $i_{dg}^{-\prime}$ and $i_{qg}^{-\prime}$ for the decoupled sequence current controller. As the positive sequence reactive current injection during faults is defined by the grid code (see Figure 22), the inverter current reference calculation in [11] is modified as below:

$$\begin{bmatrix} i_{qg}^{+}{}' \\ i_{dg}^{+}{}' \\ i_{qg}^{-}{}' \\ i_{dg}^{-}{}' \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ v_{qg}^{+} & v_{dg}^{+} & v_{qg}^{-} & v_{dg}^{-} \\ v_{qg}^{-} & v_{dg}^{-} & v_{qg}^{+} & v_{dg}^{+} \\ -v_{dg}^{-} & v_{qg}^{-} & v_{dg}^{+} & -v_{qg}^{+} \end{bmatrix}^{-1} \begin{bmatrix} i_{qg}^{'} \\ P_0 \\ P_{C2} \\ P_{S2} \end{bmatrix} \quad (23)$$

where P_0 is approximated by

$$P_0 = V_{lv}^{+}\, i_{dg}^{'} \quad (24)$$

The calculated reference values in (23) is revised considering the converter limits I_{dg}^{lim} and I_{qg}^{lim}. For example, when $\left(i_{qg}^{+}{}' + i_{qg}^{-}{}'\right) > I_{qg}^{lim}$, the q-axis reference current references are revised as below

$$\begin{aligned} i_{qg}^{+}{}'' &= i_{qg}^{+}{}' \left[\frac{I_{qg}^{lim}}{\left(i_{qg}^{+}{}' + i_{qg}^{-}{}'\right)}\right] \\ i_{qg}^{-}{}'' &= i_{qg}^{-}{}' \left[\frac{I_{qg}^{lim}}{\left(i_{qg}^{+}{}' + i_{qg}^{-}{}'\right)}\right] \end{aligned} \quad (25)$$

where I_{qg}^{+}" and I_{qg}^{-}" are the revised reference values for q-axis positive and negative currents, respectively.

The revised d-axis positive and negative current references I_{dg}^{+}" and I_{dg}^{-}" can be obtained with the same approach using I_{dg}^{lim}. It should be emphasized here that, during faults the priority is providing I_{dg}^{+} specified by the grid code. The remaining reserve in the inverter control is used for eliminating P_{C2} and P_{S2}. Hence, its performance reduces with the decrease in electrical distance between the PV park and the unbalanced fault location.

As i_{dg}^{+}, i_{qg}^{+}, i_{dg}^{-} and i_{qg}^{-} are controlled, the decoupled sequence control contains four PI regulator and requires sequence extraction for inverter currents and voltages. The sequence decoupling method [10] shown in Figure 28 is used in EMTP implementation. In this method, a combination of a low-pass filter (LPF) and double line frequency Park transform (P^{-2} and P^{+2}) is used to produce the oscillating signal, which is then subtracted. The blocks C and P represent the Clarke and Park transformation matrices, and the superscripts ±1 and ±2 correspond to direct and inverse transformation at line frequency and double line frequency, respectively.

In EMTP implementation, the feed-forward compensating terms $\left(\omega L_{choke} i_{qg} + v_{d-choke}\right)$ and $\left(-\omega L_{choke} i_{dg} + v_{q-choke}\right)$ are kept in coupled form and added to the PI regulator outputs in stationary αβ-frame.

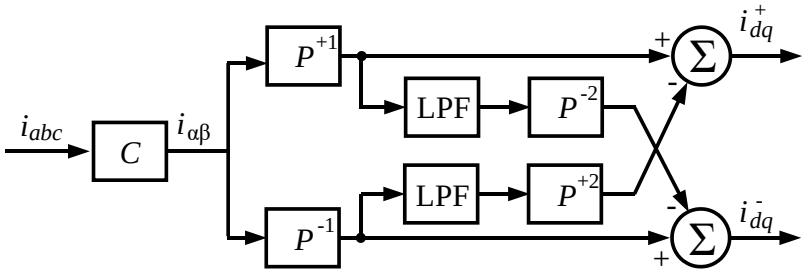


Figure 28 Sequence extraction using decoupling method [10].

3.6 Inverter protection system block

The “protection system” block includes an over/under voltage relay, deep voltage sag detector, dc overvoltage protection and an overcurrent detector for each converter to protect IGBT devices when the system is subjected to overcurrent. For initialization, all protection systems, except for DC chopper protection, are activated after 300ms of simulation (i.e. init_Prot_delay = 0.3s). The protection system parameters (except over/under voltage relay) can be modified from the device mask as shown in 2.

3.6.1 Over/under voltage protections and deep voltage sag detector

The over/under voltage protections are designed based on the technical requirements set by Hydro Quebec for the integration of renewable generation. The over/under voltage limits as a function of time are presented in Figure 29 and can be modified in the inverter device mask. The voltages below the red line reference and above the black line reference correspond to the ride-through region where the inverter is supposed to remain connected to the grid.

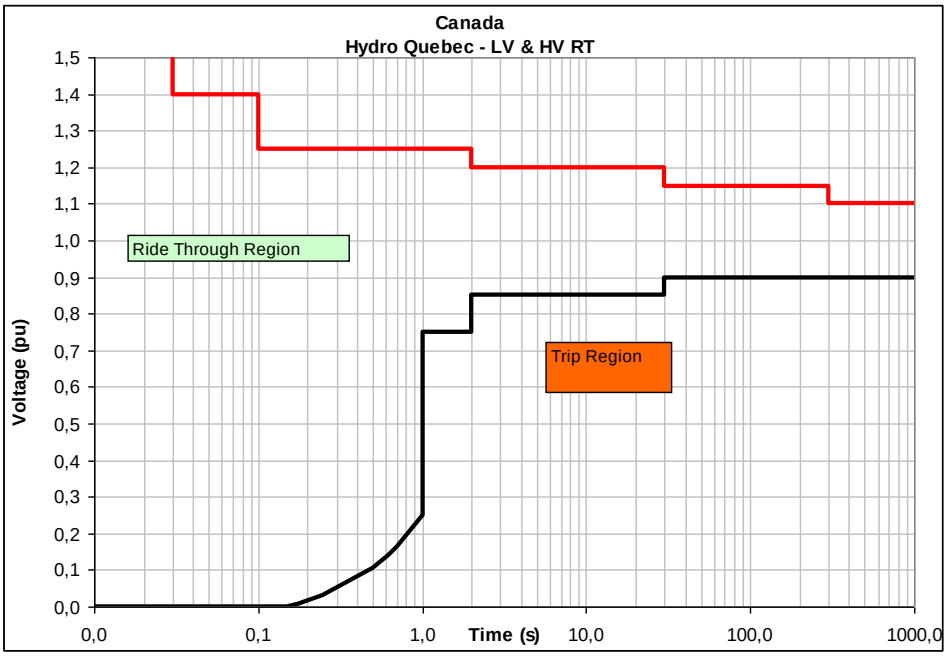


Figure 29 LVRT and HVRT requirements [12]

This block measures the rms voltages on each phase and sends a trip signal to the inverter circuit breaker when any of the phase rms voltage violates the limits in Figure 29 (see the upper part of Figure 30).

The “Deep Voltage Sag Detector” block (lower part of Figure 30) temporary blocks the Inverter in order to prevent potential overcurrent and restrict the FRT operation to the faults that occur outside the inverter.

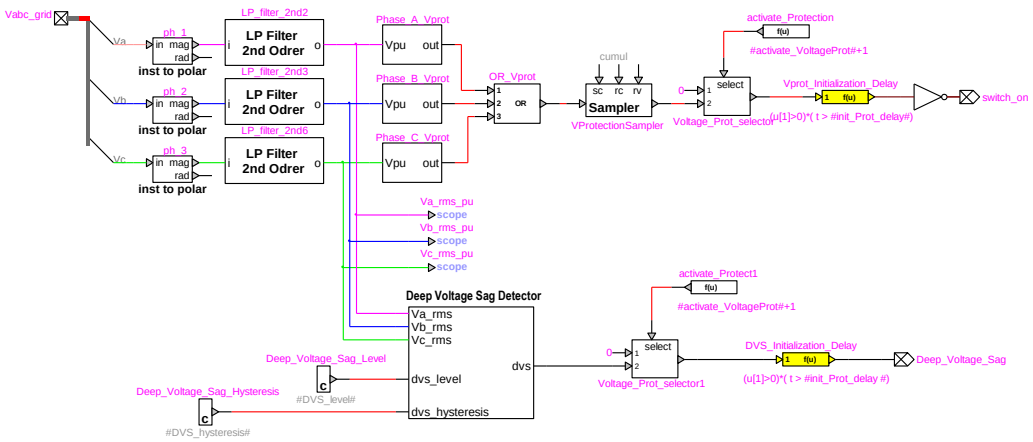


Figure 30 Over/under-voltage protections and deep voltage sag protection

3.6.2 DC overvoltage protection block

The function of DC chopper is to limit the DC bus voltage. It is activated when the dc bus voltage exceeds $|U_{chopper-ON}|$ and deactivated when dc bus reduces below $|U_{chopper-OFF}|$. EMTP diagram of the “dc overvoltage protection” is shown in Figure 31.

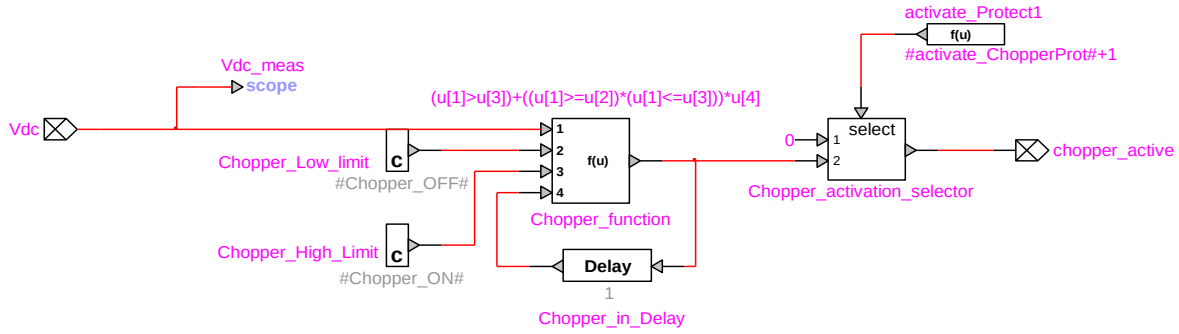


Figure 31 dc overvoltage protection block

3.6.3 overcurrent protection block

The overcurrent protection shown in Figure 32 blocks the converter temporarily when the converter current exceeds the pre-specified limit.

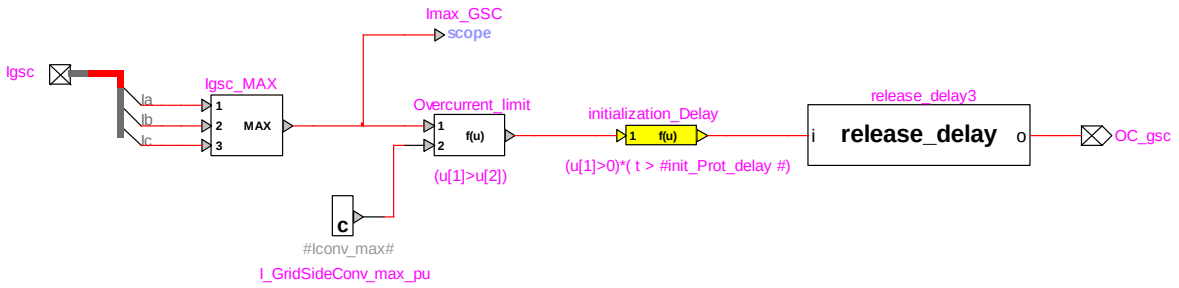


Figure 32 Overcurrent protection block

3.7 Inverter harmonic model

For harmonic analysis, the PV park is modeled with a harmonic Norton source. The harmonic study can be done in time domain, in which case **Use harmonic model for steady-state and time-domain simulations** must be checked or in the frequency domain with the frequency-scan simulation option, in which case **Use harmonic model for frequency-scan simulations**.

The harmonic currents are provided in percentage of the fundamental, for one inverter. The total park current is rescaled according to the number of inverters in service.

It is possible to automatically adjust the fundamental frequency current generated by each inverter and the harmonic current angles to match the load-flow results by checking Adjust fundamental frequency current to match Load-Flow results. When this box is checked, the I Angle input of the first line, which corresponds to the fundamental frequency current is adjusted to match the inverter current angle during the load-flow. The Fundamental frequency current magnitude is also adjusted to match the load-flow results. The fundamental frequency angle value is also added to the I Angle values of the other harmonics. Therefore, when this option is checked, the phase difference between the harmonic currents and the fundamental frequency current should be entered in the **I Angle** column.

4 Inverter Model Simulations

In this section, some simulation tests are performed to demonstrate some features of the inverter. For following tests, P and Q control type is set to the PI control, DM is used for the converter model, and control type is set to coupled control.

4.1 Load flow and flat start simulation

During the first 0.2s of simulation, an ideal voltage source maintaining the voltage angle and magnitude calculated during Load-Flow is connected to the inverter PPC. It allows the park controls to initialize. After this time, the ideal voltage source is disconnected, and the active and reactive powers hold.

Figure 33 and Figure 34show the flat start test results for active power references of 45MW (1pu), and reactive power reference of 0MVAR. The load-flow results match very well the references and the model initializes correctly with no warning or error messages.

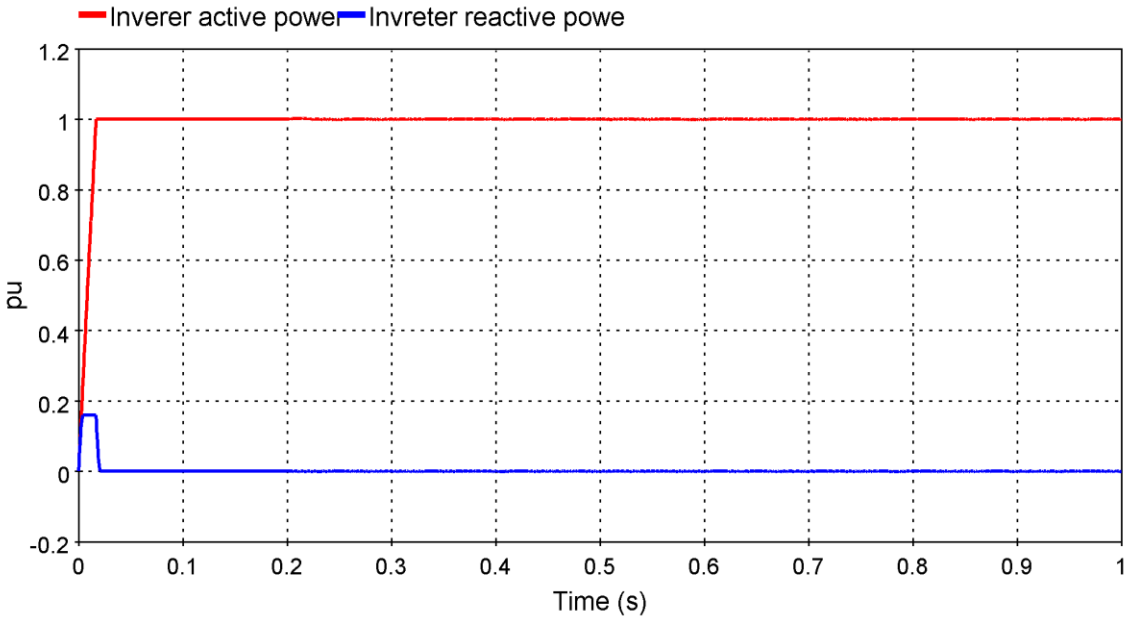


Figure 33 Initialization and flat start test: inverter active and reactive power

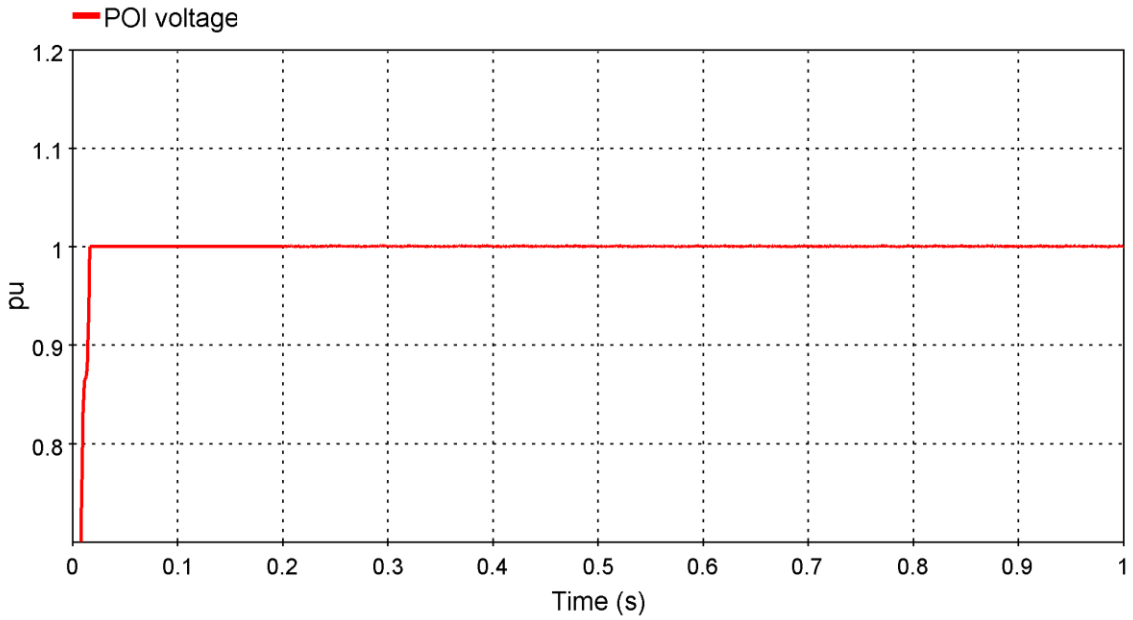


Figure 34 Initialization and flat start test: RMS voltage at POI

4.2 Active power control

In this simulation, several active power reference steps are applied to Pref input. Initially, the inverter generates 45MW (1pu) and 0MVAR.

Figure 35 shows the active power follows the reference changes. During a active power reference step change, the inverter reaches 90% of the new setpoint value in less than 0.1 seconds and the error between the inverter active power and the reference is less than 1% after 0.3 seconds.

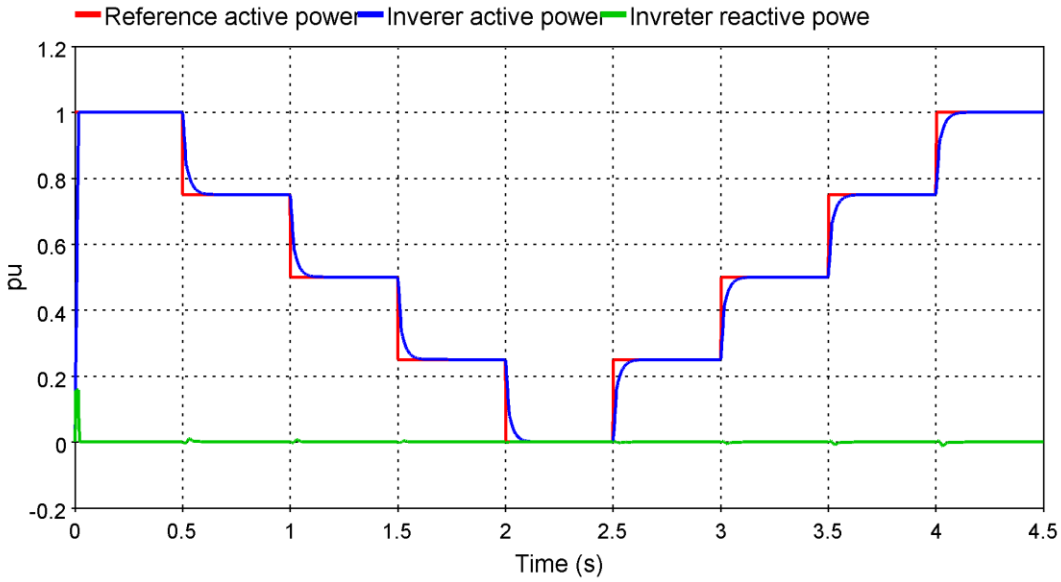


Figure 35 Active power control test: reference active power, inverter active power, inverter reactive power

4.3 Reactive power control

In this simulation, several reactive power reference steps are applied to Pref input. Initially, the inverter generates 40.5MW (0.9pu) and 0MVAR.

Figure 35 shows the reactive power follows the reference changes. During a reactive power reference step change, the inverter reaches 90% of the new setpoint value in less than 0.1 seconds and the error between the inverter reactive power and the reference is less than 1% after 0.3 seconds.

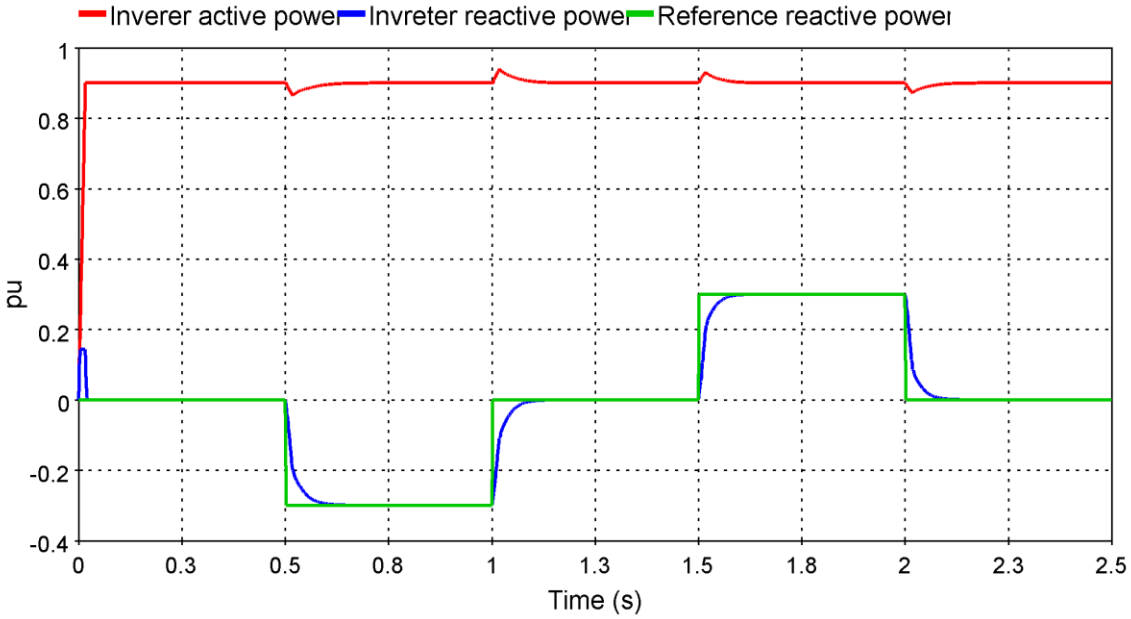


Figure 36 Reactive power control test: reference reactive power, inverter active power, inverter reactive power

4.4 LVRT test

This test presents the model response during LVRT. A three-phase fault with fault impedance of 0.5Ω is applied at POI. Fault duration is 0.5s, and the inverter initially generates 45MW and 0MVAR.

Figure 37 shows the voltage at POI point, and Figure 38 shows inverter active and reactive power. The inverter stays connected to the grid while providing current support during LVRT.

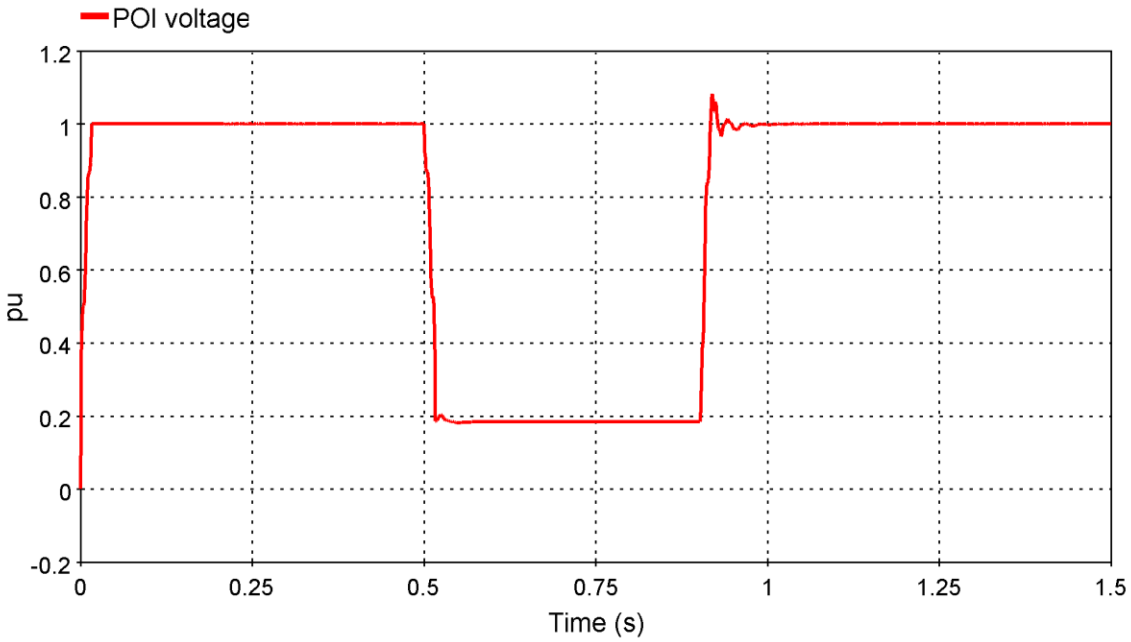


Figure 37 LVRT test: RMS voltage at POI

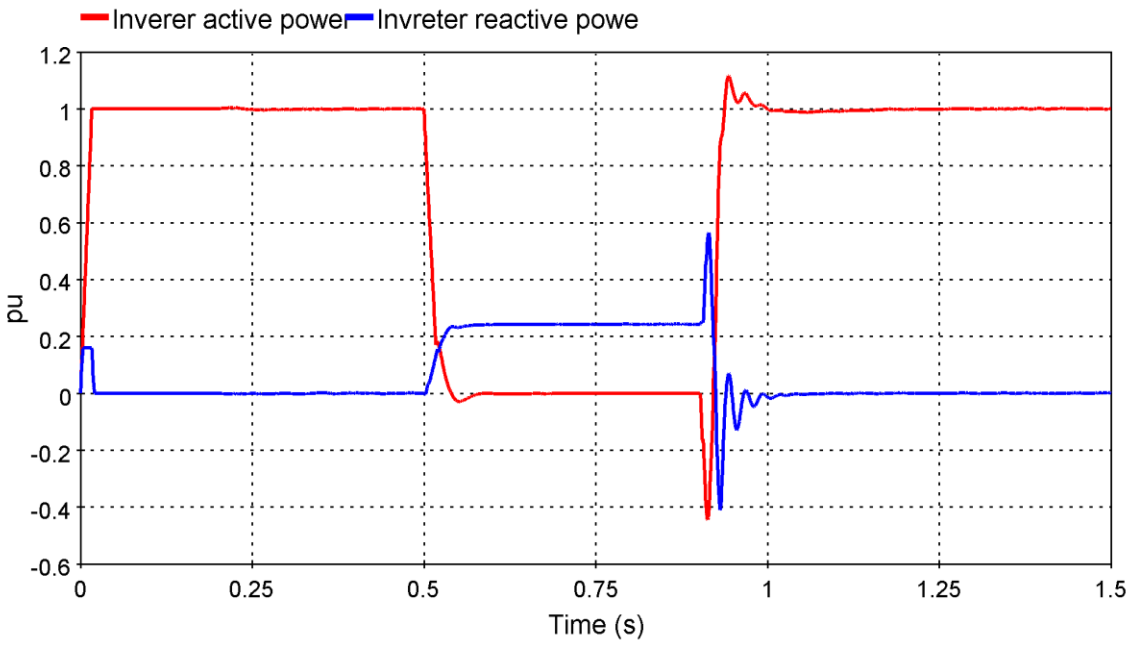


Figure 38 LVRT test: inverter active power, inverter reactive power

5 References

[1] M. P. K. a. L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," *IEEE Transactions on Industrial Electronics,* vol. 45, pp. 691-703, 1998.

[2] A. Yazdani and R. Iravani, Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications, Wiley-IEEE Press, 2010.

[3] J. M. N. X. Z. L. a. G. C. V. S. R. Sanders, "Generalized averaging method for power conversion circuits," in *ual IEEE Conference on Power Electronics Specialists* , San Antonio, TX, USA,, 1990.

[4] H. P. a. W. L. K. J. G. Slootweg, "Representing wind turbine electrical generating systems in fundamental frequency simulations," *IEEE Transactions on Energy Conversion,* vol. 18, no. 4, pp. 516-524, 2003.

[5] G.-C. H. a. J. C. Hung, "Phase-locked loop techniques. A survey," *IEEE Transactions on Industrial Electronics,,* vol. 43, no. 6, pp. 609-615, 1996.

[6] R. T. M. L. a. A. V. T. F. Blaabjerg, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics,* vol. 53, no. 5, pp. 1398-1409, 2006.

[7] U. K. e. al, "A Generic EMT-Type Model for Wind Parks With Permanent Magnet Synchronous Generator Full Size Converter Wind Turbines," *IEEE Power and Energy Technology Systems Journal,* vol. 6, no. 3, pp. 131-141, Sept. 2019.

[8] L. H. a. H. Nee, "Model-based current control of ac machines using the internal model control," *IEEE Transactions on Inductrial Application,* pp. 133-141, 1998.

[9] "Grid code - high and extra high voltage," E.ON Netz GmbH, Bayreuth, Germany, April 2006.

[10] J. P. J. B. J. I. C. R. P. B. a. D. B. P. Rodriguez, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," *ansactions on Power Electronics,* vol. 22, no. 2, pp. 584-592, March 2007.

[11] R. Teodorescu, M. Liserre and P. Rodriguez, Grid Converters for Photovoltaic and Wind Power Systems, Wiley-IEEE Press, 2007.

[12] "Transmission Provider Technical Requirements for the Connection of Power Plants to the Hydro-Quebec Transmission System," Hydro Quebec Transenergie, 2009.