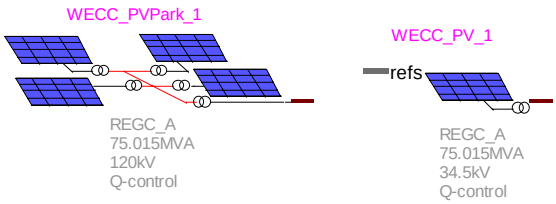
WECC PV park



Hossein Ashourian, Henry Gras, 5/5/2023 5:46 PM

1 Description

This document presents a generic EMTP PV park model. The PV inverter control systems are mainly intended to implement the models suggested by Renewable Energy Modeling Task Force of the Western Electric Coordinating Council (WECC) [1]- [2] in EMTP. Here, it is named the WECC PV park model. The WECC PV park model contains three main controllers:

- The renewable energy generator controller (REGC),
- The renewable energy electrical controller (REEC), and
- The renewable energy plant controller (REPC).

To interfaces the power converter to the external grid the converter can be modeled as

- Detailed (DM), in which a detailed circuitry of the power converter is implemented in EMTP including power semiconductors (e.g., IGBT switches), DC bus, measuring filters etc. [3] [4],
- Average-Value (AVM), in which power semiconductor switches are replaced by average value model of the inverter replicating the average response of switching devices, converters and controls [3] [4], or
- a voltage source, in which the direct-current (DC) bus is neglected. The converter/generator controller is developed based on the REGC_C model [1] in EMTP, or
- a current source, in which the DC bus is neglected. The converter/generator controller is model based on the REGC_A model [2] in EMTP.

For DM or AVM, the inverter model is a three-phase grid-connected voltage source converter (VSC). The voltage references for the inverter/converter are calculated by the inner current loops using dq-frame decoupling feed-forward technique [3], [4]. The DC link of the converter is connected to a constant DC voltage source. The constant DC voltage source can be replaced with a photovoltaic (PV) module or a battery energy storage system (BESS). Therefore, the dynamic of the voltage on the DC bus during the AC grid faults or device failures/malfunctions can be observed and analysed.

For REGC_C and REGC_A based models, the converter hardware is modeled with voltage and current sources respectively. These are mainly developed in EMTP to import the advanced models, to run different control algorithms, and to compare the EMT results from/with ones used in the positive-sequence power system software platforms such as General Electric GE-PSLF, Siemens PTI PSSE, PowerWorld simulator, and PowerTech Labs TSAT. Besides, both balance and unbalance conditions can be simulated in EMTP which is not commonly used in these platforms.

AVM, REGC_C and REGC_A models have the advantage of using much higher the simulation integration time step compared to the detailed model (DM), therefore significantly reducing the simulation time. A time-step of 10μs or smaller for the DM, a time-step of 20μs or smaller for the AVM, and a time-step of 100μs or smaller for the REGC_C and REGC_A models can be used in the EMTP simulations.

REEC controller represents the outer control loops of the inverter. It receives the active and reactive power reference from the REPC module, with feedback of terminal voltage and generator power output, calculates reference active and reactive currents, and sends real and reactive current commands to the inner current loops or the REGC controllers. In EMTP, REEC_D model is implemented [2]. This is the most recent inverter control model developed by WECC, which contains new features, such as extended voltage-dependent current limit tables (VDLp, VLDq curves), local current compensation, local reactive-droop compensation, reactive-current injection algorithm, model inverter blocking logic etc. REEC_A or REEC_B models (older versions) can be converted to REEC_D with modifying some parameters [5]. It can be used to model wind, PV and BESS.

REPC controller represents the park controller model. It monitors the point of interconnection (POI) of a plant and sends real and reactive power commands to PV inverters in the plant to control the real power and reactive power/voltage/power factor at the POI. In EMTP, REPC_A model is implemented which is the original simple plant level controller [2].

The park model includes the collector system of the plant, converter transformer, and park transformer. The converter model including the converter transformer and the collector system are aggregated. The converter and the control systems include the necessary nonlinearities, transient and protection functions to simulate accurately the transient and dynamic behavior of the converter to external power system disturbances.

The control system models can run from a compiled code. The simulation speed increases when the model run from the compiled code.

The model is an open source and a flexible model. User can easily modify the control block diagrams and adapt the control parameters according to the specified design used in the PV park plant. The model is valid for load-flow, time-domain, and frequency scan simulation types.

2 PV park Pins and Device Mask

The section describes the converter pins and device mask.

2.1 PV park pins

This device has 2 pins:

Table 1 PV park model Pins

Pin name	Port type	Description	Units
PCC	3-phase power	Point of Common Coupling	

2.2 Parameters

2.2.1 General tab

- **Number of aggregated inverters:** number of parallel-connected PV arrays or inverters.
- **Frequency:** grid frequency.
- **Collector grid nominal AC voltage:** voltage on the collector grid.
- **Transmission grid nominal AC voltage:** voltage on the transmission grid.
- **Including zig-zag transformer on the collector grid:** if this option is checked, a zig-zag transformer is added on LV side of the park transformer.
- $\boldsymbol{R_0}$**:** primary winding resistance of the zig-zag transformer
- $\boldsymbol{L_0}$**:** primary winding inductance of the zig-zag transformer
- **PV array/inverter rated power:** rated apparent power of a single inverter.
- **Inverter nominal voltage:** nominal voltage of inverter.
- **DC voltage:** DC-link voltage.
- **Filter reactive power:** reactive power generated by each inverter harmonic filter. See 3.2.3 for more information on the filter.
- **Choke resistance:** choke resistance.
- **Choke inductance:** choke inductance.
- **Include equivalent collector grid:** if this option is checked, an equivalent PI model collector grid is added between inverter transformer and park transformer.
- **Equivalent resistance:** collector grid equivalent resistance.
- **Equivalent inductance:** collector grid equivalent inductance.
- **Equivalent capacitance:** collector grid equivalent capacitance.
- **Number of inverters in service:** number of parallel-connected arrays/inverters in service.

- **Q-control mode:** Q-control, V-control or PF-control.
  Note: this parameter regulates reactive power or voltage, or power factor at POI.
- **Reactive power reference:** reactive power reference at point of interconnection.
- **Voltage reference:** voltage reference at point of interconnection.
- **Power factor reference:** power factor reference at point of interconnection.
- **Active power reference:** active power reference at point of interconnection.

2.2.2 Park Transformer tab

The 'Nominal three-phase nameplate input' transformer model from the standard EMTP library is used.

- **Connection Type:** see options.
- **Nominal power:** nominal power of a single transformer.
- **Nominal frequency:** nominal frequency of the transformer.
- **Grid side voltage:** nominal voltage transformer on the grid side.
- **Inverter side voltage:** nominal voltage transformer on the inverter side.
- **Winding R:** winding resistance.
- **Winding X:** winding reactance.
- **Winding impedance on winding 1:** distribution ratio
- **Magnetization data:** current-flux data.
- **Magnetization resistance:** magnetization resistance.
- **Exclude magnetization branch model:** if this option is checked, the magnetization branch model is excluded.

2.2.3 Inverter Transformer tab

The 'Nominal three-phase nameplate input' transformer model from the standard EMTP library is used.
In the converter transformer tab, the data must insert for the one converter transformer. The converter model is aggregated. Therefore, the converter transformer is aggregated according to number of aggregated converters, which is automatically done by a script. The total nominal power of one aggregated converter transformer is equal to one converter transformer nominal power multiplied by the number of aggregated converters.

- **Connection Type:** see options.
- **Nominal power:** nominal power of a single transformer.
- **Nominal frequency:** nominal frequency of the transformer.
- **Grid side voltage:** nominal voltage transformer on the grid side.
- **Inverter side voltage:** nominal voltage transformer on the inverter side.
- **Winding R:** winding resistance.
- **Winding X:** winding reactance.
- **Winding impedance on winding 1:** distribution ratio.
- **Magnetization data:** current-flux data.
- **Magnetization resistance:** magnetization resistance.
- **Exclude magnetization branch model:** If this option is checked, the magnetization branch model is excluded.

2.2.4 Converter Control tab

- **Converter model:** It can be either
  DM, detailed model + generic current control model,
  AVM, average value model + generic current control model,
  current source + REGC_A model, or
  voltage source + REGC_C model.
- **Use compiled code for the data acquisition:** using complied code will increase the simulation speed.
- **Use compiled code for the inverter control system:** using complied code will increase the simulation speed.

2.2.4.1 AVM or DM converter models

- **PWM frequency:** PWM frequency
- **PLL K_i:** PLL PI controller, integral gain.
- **PLL K_p:** PLL PI controller, proportional gain.
- **Current loop PI controller parameters:** PI controller gains or rise time.
- **PI controller K_i:** PLL PI controller, integral gain
- **PI controller K_p:** PLL PI controller, proportional gain.
- **Rise time:** closed-loop current control rise-time.
- **R_{sys}:** equivalent resistance of the external network.
- **X_{sys}:** equivalent reactance of the external network.
- **Sampling rate:** sampling rate frequency.
- **Measuring input filter type:** Bessel or Butterworth.
- **Measuring input filter order**
- **Cutoff frequency:** cutoff frequency of measuring input filters.
- **Rate flag switch**: ramp rate limit on active current or active power.
- **Voltage filter time constant T_{filtr}:** filter time constant for voltage measurement.
- **Upper ramp rate limit I_{qrmax}:** maximum rate at which a reactive current recover after a fault.
- **Lower ramp rate limit I_{qrmin}:** minimum rate at which a reactive current recover after a fault.
- **Ramp rate limit for active power $rrpwr$:** rate a which active current (power) recovers after a fault.

2.2.4.2 REGC_A converter model

- **Low Voltage Power Logic:** low voltage power limiter (LVPL) logic is enabled when flag Lvplsw is set 1.
- **Converter time constant T_g:** converter current regulator lag time constant.
- **Active current ramp rate limit Rrpwr:** active current up-ramp rate limit on voltage recovery.
- **LVPL characteristic voltage 2 Brkpt:** LVPL breakpoint voltage.
- **LVPL characteristic voltage 1 Zerox:** LVPL zero crossing voltage.
- **LVLP gain Lvpl1:** LVPL gain.
- **Voltage limit Volim:** voltage limit in high voltage reactive current.
- **High voltage point Lvpnt1:** high voltage point for low voltage active current management.
- **Low voltage point Lvpnt0:** low voltage point for low voltage active current management.
- **Current limit Iolim:** limit in high voltage reactive current management.
- **Voltage filter time constant Tfiltlr:** terminal voltage filter time constant for low voltage active current management.
- **Overvoltage compensation on gain Khv:** overvoltage compensation or gain Acceleration factor (Accel) used in the high voltage reactive current management.
- **Upper limit Iqrmax:** upper limit on rate of change for reactive current.
- **Lower limit Iqrmin:** lower limit on rate of change for reactive current.

Voltage angle measurement

- **Proportional-gain Kppll:** PLL PI controller, proportional gain
- **Integral gain Kipll:** PLL PI controller, integral gain
- **Upper limit wmax:** PLL PI controller, upper limit.
- **Lower limit wmin:** PLL PI controller, lower limit.

2.2.4.3 REGC_C converter models

- **Rate flag switch:** ramp rate limit on active current or active power.
- **Upper ramp rate limit I_{qrmax}:** maximum rate at which a reactive current recover after a fault.

- **Lower ramp rate limit I_{qrmin}:** minimum rate at which a reactive current recover after a fault.
- **Voltage filter time constant T_{filtr}:** filter time constant for voltage measurement.
- **Ramp rate limit for active power $rrpwr$:** rate a which active current (power) recovers after a fault.
- **Time constant T_e:** filter time constant to model inner control loops.
- **Proportional-gain Kip:** inner current loop PI controller, proportional gain
- **Integral gain Kii:** inner current loop PI controller, integral gain
- **Proportional-gain Kppll:** PLL PI controller, proportional gain
- **Integral gain Kipll:** PLL PI controller, integral gain
- **Upper limit wmax:** PLL PI controller, upper limit.
- **Lower limit wmin:** PLL PI controller, lower limit.

2.2.4.4 REEC_D control model

- **Power factor control PfFlag:** power factor control or Q control (which can be controlled by an external signal)
- **Voltage/Q control VFlag:** Q control or voltage control
- **Voltage/Q/PF control QFlag:** voltage or Q control, or constant pf or Q control
- **P dependency PFlag:** active current command has speed dependency or no dependency (always set to 0 for solar PV plant)
- **P/Q priority Pqflag:** reactive power priority or active power priority
- **Q compensation Vcmpflag:** use current compensation or use reactive droop
- **Baseload flag:** Normal operation, or PMAX= initial power (Pgen0), or PMAX=PMIN=Initial power (Pgen0).
- **Low voltage threshold Vdip:** low voltage condition trigger voltage.
- **High voltage threshold Vup:** high voltage condition trigger voltage.
- **Time constant Trv:** terminal bus voltage filter time constant.
- **Gain Kqv:** Reactive current injection gain during over and undervoltage conditions.
- **Overvoltage deadband dbd1:** overvoltage deadband for reactive current injection (≤ 0).
- **Undervoltage deadband dbd2:** undervoltage deadband for reactive current injection (≥ 0).
- **Upper limit Iqh1:** maximum reactive current injection.
- **Lower limit Iql1:** minimum reactive current injection.
- **Voltage reference Vref0:** reference voltage for reactive current injection (if 0, model initializes it to initial terminal voltage automatically).
- **Constant Iqfrz:** value at which Iqinj is held for thld seconds following a voltage dip event.
- **Time delay Thld:** time delay associated with Iqinj when voltage_dip is reset from 1 to 0:
  a) If Thld = 0, no other action is taken.
  b) If Thld > 0, then for Thld seconds following a voltage dip (i.e. voltage_dip goes from 1back to 0) Iqcmd_bl is held at its current value (i.e. value just prior to the end of the voltage_dip) for Thld seconds and is then released.
  c) If Thld < 0, then for Thld seconds following a voltage dip (i.e. voltage_dip goes from 1 back to 0) Iqcmd_bl is held equal to Iqfrz for Thld seconds and is then released.
- **Time delay Thld2:** time delay that active current command is held/frozen at the previous value for Thld2 seconds following a voltage dip, i.e. voltage_dip goes from 1 back to 0
- **Upper limit Qvmax:** maximum value of the incoming Qext or Vext (≥ 0).
- **Lowe limit Qvmin:** minimum value of the incoming Qext or Vext (≤ 0).
- **Upper limit VMAX:** maximum voltage at inverter terminal bus (≥ 0).
- **Lower limit VMIN:** minimum voltage at inverter terminal bus (≤ 0).
- **Proportional gain Kqp:** local reactive power regulator proportional gain.
- **Integral gain Kqi:** local reactive regulator integral gain.
- **Proportional gain Kvp:** local voltage regulator proportional gain.
- **Integral gain Kvi:** local voltage regulator integral gain.
- **Voltage reference Vref1:** inner-loop voltage control reference. Note: this parameter is a user defined parameter which is added to “refs” input bundle.

- **Time constant Tiq:** reactive current regulator lag time constant.
- **Up_ramp limit dPmax:** active power up-ramp limit (>0).
- **Down_ramp limit dPmin:** active power down-ramp limit (>0).
- **Upper limit PMAX:** maximum active power.
- **Lower limit PMIN:** minimum active power.
- **Time constant Tp:** active power filter time constant.
- **Time constant Tpord:** inverter power order lag time constant.
- **Compensation resistance rc:** current-compensation resistance.
- **Compensation reactance Xc:** current-compensation reactance.
- **Time constant Tr1:** filter time constant for voltage measurement. It can be set to “zero”.
- **Compensation gain Kc:** reactive-current compensation gain.
- **Low voltage threshold Vblkl:** voltage below which the converter is blocked (i.e. Iq = Ip = 0).
- **High voltage threshold Vblkh:** voltage above which the converter is blocked (i.e. Iq = Ip = 0).
- **Time delay Tblk:** the time delay following blocking of the converter after which the converter is released from being blocked.
- **Scaling gain Ke:** Scaling on Ipmin; set to 0 for a generator, set to a value between 0 and 1 for a storage device, as appropriate.
- **Maximum current Imax:** maximum apparent current.
- **VDLq data:** 12 pairs of values defining the voltage dependent reactive-current limits. Voltage versus reactive-current curve for VDLq data.
- **VDLp data:** 12 pairs of values defining the voltage dependent active-current limits. Voltage versus active-current curve for VDLp data.

2.2.5 Protection tab

2.2.5.1 Voltage sag protection

- **Enable:** if this option is checked, the voltage sag protection is enabled.
- **Pickup DVS voltage:** threshold voltage value to activate the Deep-Voltage-Sag (DVS) protection.
- **Reset DVS voltage**: threshold voltage value to deactivate the Deep-Voltage-Sag protection.

2.2.5.2 Chopper protection

- **Enable**: if this option is checked, the chopper protection is enabled.
- **Pickup** V_{DC} : chopper is ON when dc-voltage is above this value.
- **Reset** V_{DC} : chopper OFF when dc-voltage is below this value.

2.2.5.3 Overcurrent protection

- **Inverter pickup current**: converter overcurrent protection threshold.
- **Reset delay**: overcurrent protection release delay.

2.2.5.4 AC undervoltage protections

- **Enable**: if this option is checked, the AC undervoltage protection is enabled.
- **AC undervoltage protection data**: voltage versus time curve for the AC undervoltage protection.

2.2.5.5 AC overvoltage protections

- **Enable**: if this option is checked, the AC overvoltage protection is enabled.
- **AC overvoltage protection data**: voltage versus time curve for the AC overvoltage protection.

2.2.6 Park controller tab

2.2.6.1 Q/V control

- **Voltage droop control VCFlag**: reactive droop or line drop compensation.
- **Time constant Tfltr:** voltage and reactive power filter time constant.
- **Proportional gain Kp:** Volt/VAr regulator proportional gain.
- **Integral gain Ki:** Volt/VAr regulator integral gain.
- **Lead time constant Tft:** plant controller Q output lead time constant.
- **Lag time constant Tfv:** plant controller Q output lag time constant.
- **Voltage Vfrz:** voltage for freezing Volt/VAr regulator integrator.
- **Compensation resistance Rc:** line drop compensation resistance.
- **Compensation reactance Xc:** line drop compensation reactance.
- **Compensation gain Kc:** reactive droop gain.
- **Upper limit emax:** maximum Volt/VAr error.
- **Lower limit emin:** minimum Volt/VAr error.
- **Lower threshold for deadband dbd1:** reactive power lower threshold deadband.
- **Upper threshold for deadband dbd2:** reactive power upper threshold deadband.
- **Upper limit Qmax:** maximum plant reactive power command.
- **Lower limit Qmin:** minimum plant reactive power command.

2.2.6.2 P/frequency control

- **Frequency control Fflag:** governor response disable or enable.
- **Proportional gain Kpg:** real power control proportional gain.
- **Integral gain Kig:** real power control integral gain.
- **Time constant Tp:** active power filter time constant.
- **Lower threshold deadband fdbd1:** frequency deadband downside.
- **Upper threshold deadband fdbd2:** frequency deadband upside.
- **Upper limit femax:** maximum power error in droop regulator.
- **Lower limit femin:** minimum power error in droop regulator.
- **Upper limit Pmax:** maximum plant active power command.
- **Lower limit Pmin:** minimum plant active power command.
- **Time constant Tg**: plant controller P output lag time constant.
- **Over-frequency droop Ddn:** reciprocal of down regulation droop.
- **Under-frequency droop Dup:** reciprocal of up regulation droop.

2.2.7 Harmonics tab

- **Use harmonic model for steady-state and time-domain simulations**: if this option is checked, this device is modeled as a harmonic current source for steady-state and time-domain simulations.
- **Use harmonic model for frequency-scan simulations**: if this option is checked, the Fundamental frequency current magnitude input and the first line of the Harmonic data table are adjusted to match the load-flow solution current.
- **Adjust fundamental frequency current to match load-flow solution results**: if this option is checked, this device is modeled as a harmonic current source during Frequency scan simulations.
- **Fundamental frequency current magnitude (for one inverter)**: magnitude of the fundamental frequency current for 1 inverter in A RMS. This value is automatically multiplied by the number of inverters in service.
- **Harmonics data table**: harmonic contents for phase-a (balanced source).

3 WECC PV park model

3.1 General

The general structure of the PV park model is shown in Figure 1. It is composed of

- o "Hardware" block which contains the PV panel and the inverter,
- o "Converter Control" block,
- o "Power Plant Controller (PPC)" block,
- o PI circuit that represents equivalent collector grid,
- o converter transformer (converter_transformer),
- o park transformer,
- o initialization Sources with load flow (LF) constraint, and
- o a Norton harmonic source for harmonic analysis.

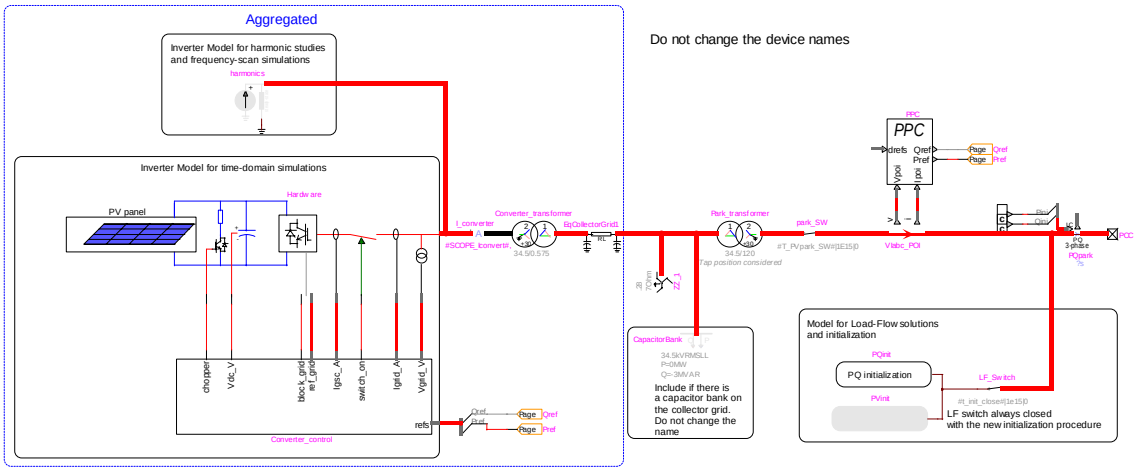


Figure 1 General structure of WECC PV park model

The PV Park content is automatically modified according to the simulation type, so the model is valid for any simulation options EMTP offers.
During load-flow, the converter is modelled by a PQ load-flow bus. The load-flow power is the *Initial active power* input, the reactive power is the *Initial reactive power input*.
In time-domain, the model is initialized with the load-flow conditions and the outer loop control initial references are the ones used during load-flow, which were detailed in the section hereabove. The initialization time is t_init =0.05s. During this time, an ideal voltage source is connected to the converter 3-phase pin. This voltage source holds the load-flow conditions while the converter controls are initializing. After this time, the ideal voltage source is disconnected by a switch.
During frequency-scan analysis, the converter hardware and converter control system is replaced a Norton harmonic source. It is connected to the low-voltage side of the converter transformer if the latter is included. No control is included when the harmonic representation is selected.
The PV Park model is an aggregated model, and it is aggregated according to the number of PV arrays/inverters (see Figure 1 aggregated zone).

3.2 Hardware

Figure 2 shows the inverter hardware in EMTP. The inverter hardware is composed of a DC-AC converter, a series RL branch (choke filter), two shunt ac harmonic filters, and the current and voltage measurement units used for monitoring and control purposes. All variables are monitored as instantaneous values and meter locations are shown in Figure 2. The inverter/generator/converter model can be

- o detailed model (DM),
- o average value model (AVM),
- o current source, or
- o voltage source.

For DM and AVM, the inverter is model as current controlled voltage source inverter, which the output current of the inverter is regulated by controlling of the voltage of the inverter. The DC resistive chopper limits the DC bus voltage and is controlled by the protection system block. This option uses when the DC bus is connected to PV or battery systems.
There is no DC bus for simple controlled voltage/current sources, therefore, the dynamic impact of the DC link on the converter/park performance is neglected. Also, the inverter is considered as an ideal power inverter generating a sinusoidal voltage/current without harmonics.

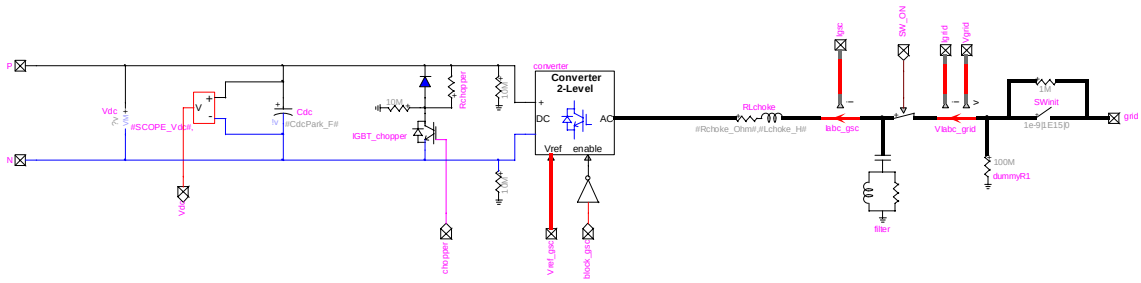


Figure 2 Inverter hardware.

3.2.1 DC-AC converter model: detailed model (DM) and average value model (AVM)

The EMTP diagram of the detailed model (DM) is shown in Figure 3. It includes a two-level voltage source converter (VSC) block and a pulse width modulation (PWM) block.
A detailed two-level topology (Figure 4.a) is used for the VSC in which the valve is composed by one IGBT switch, two non-ideal (series and anti-parallel) diodes and a snubber circuit as shown in Figure 4.b. The non-ideal diodes are modeled as non-linear resistances.
The PWM block receives the three-phase reference voltages from converter control and generates the pulse pattern for the six IGBT switches by comparing the voltage reference with a triangular carrier wave. In a two-level converter, if the reference voltage is higher than the carrier wave then the phase terminal is connected to the positive DC terminal, and if it is lower, the phase terminal is connected to the negative DC terminal. The EMTP diagram of the PWM block is presented in Figure 5.

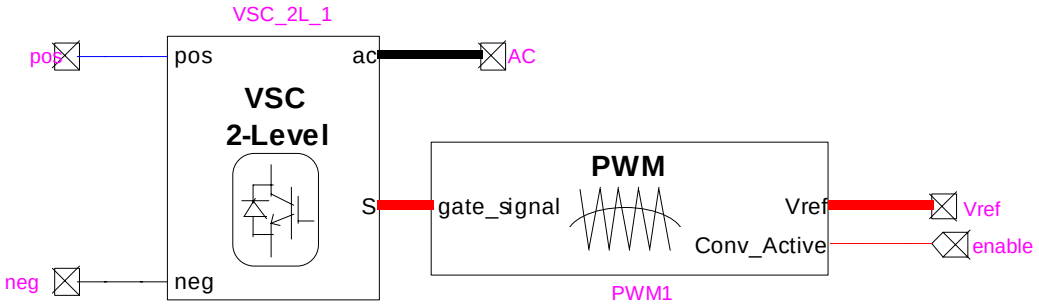


Figure 3 DC-AC converter block inside the inverter hardware model (detailed model version).

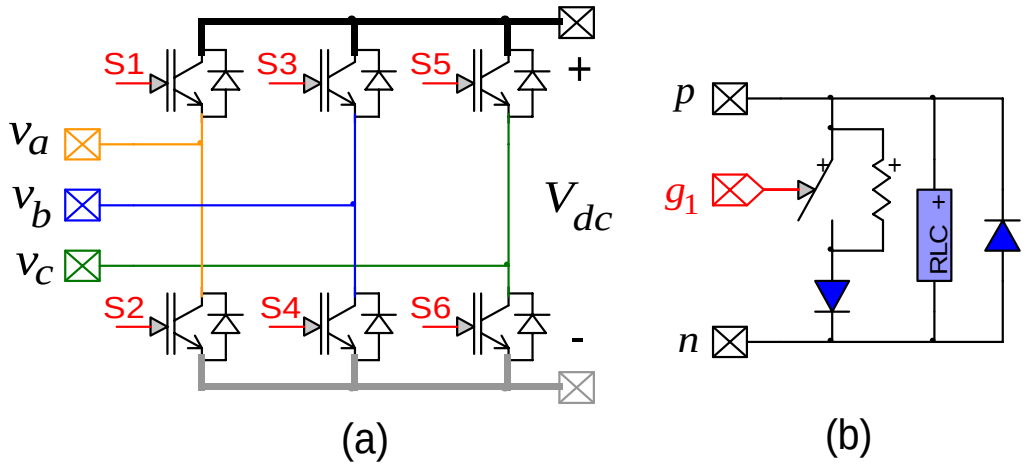


Figure 4 **(a) Two-level Converter, (b) IGBT valve.**

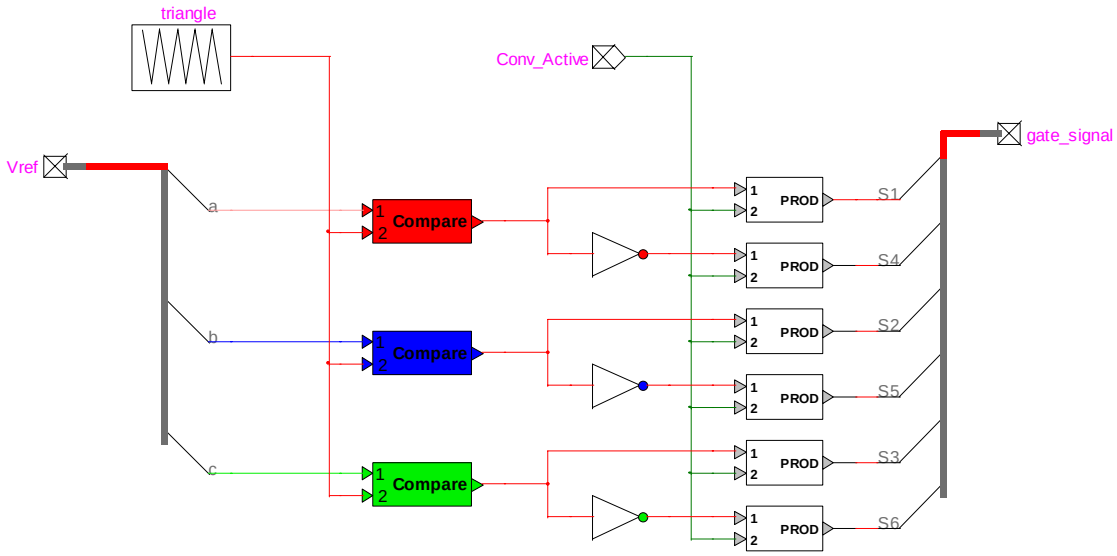


Figure 5 **PWM control block**

The DM mimics the converter behavior accurately. However, simulation of such switching circuits with variable topology requires many time-consuming mathematical operations and the high frequency PWM signals force small simulation time step usage. These computational inefficiencies can be eliminated by using average value model (AVM) which replicates the average response of switching devices, converters and controls through simplified functions and controlled sources [6] AVMs have been successfully developed for inverter-based technologies [7]. AVM obtained by replacing DM of converters with voltage-controlled sources on the AC side and current-controlled sources on the DC side as shown in Figure 6.
The fourth (converter control) tab of the inverter device mask (see Section 2.2) enables used AVM-DM selection.

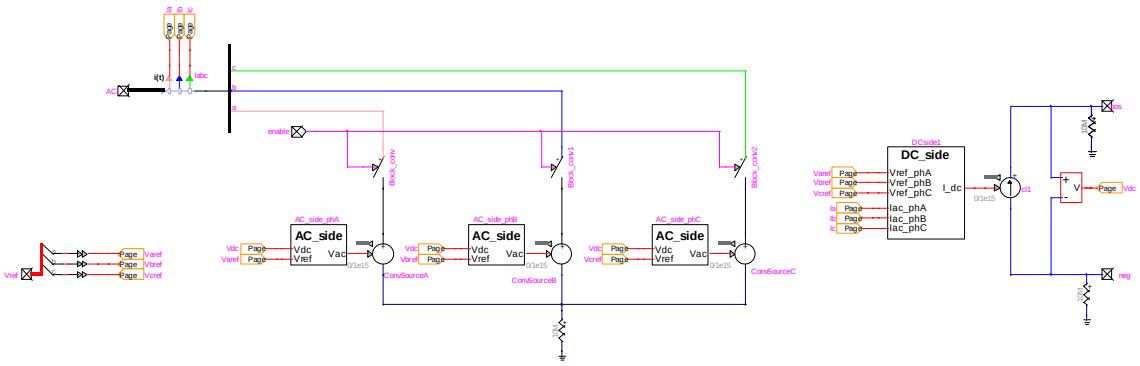


Figure 6 AVM Representation of the VSC.

3.2.2 AC converter model: voltage/current sources

These models are implemented to support the REGC_A and REGC_C models as shown in Figure 7and Figure 8.

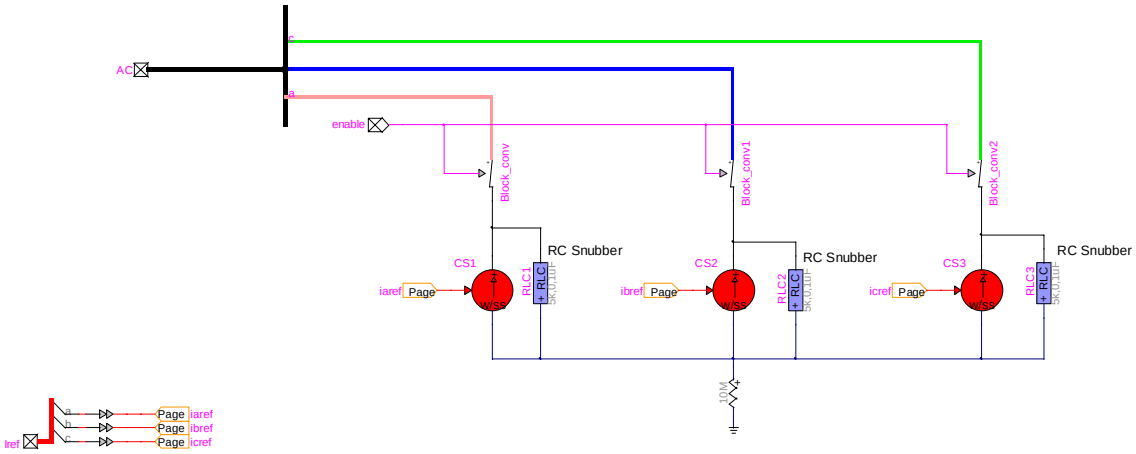


Figure 7 Current source model to support REGC_A model.

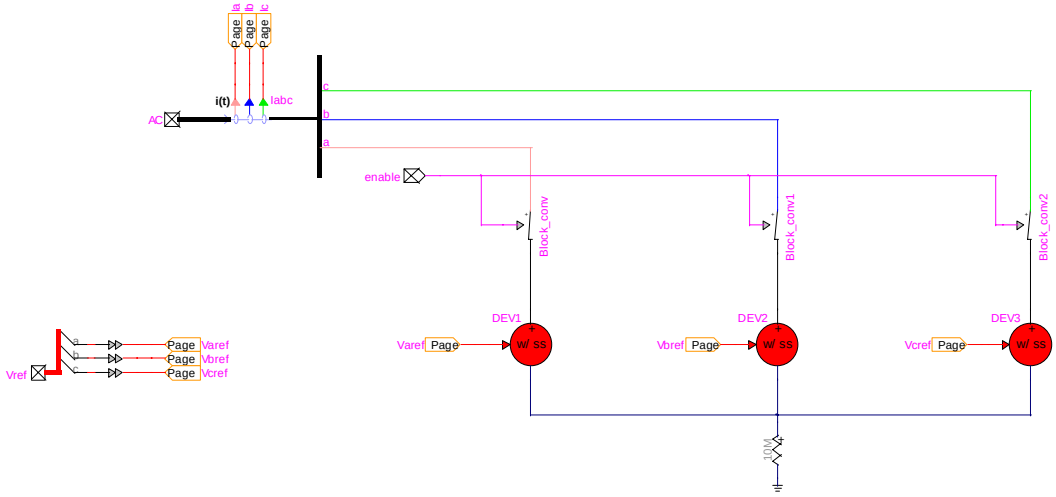


Figure 8 Voltage source model to support REGC_C model.

3.2.3 Shunt AC harmonic filters

The “shunt AC harmonic filters” block includes two harmonic filters as shown in Figure 9. These filters are tuned at switching frequencies harmonics n1 and n2. The filter parameters are computed as

$$C_{f1} = \frac{Q_{filter}\ N_{Inv}}{U^2(2\pi f)} \quad (1)$$

$$L_{f1} = \frac{N_{Inv}}{C_{f1}(2\pi f\, n_1)^2} \quad (2)$$

$$R_{f1} = \frac{(2\pi f) n_1\ L_{f1}\ Q}{N_{Inv}} \quad (3)$$

$$C_{f2} = C_{f1} \quad (4)$$

$$L_{f2} = \frac{N_{Inv}}{C_{f2}(2\pi f\, n_2)^2} \quad (5)$$

$$R_{f2} = \frac{(2\pi f) n_2\ L_{f2}\ Q}{N_{Inv}} \quad (6)$$

where U is the rated LV grid voltage, Q_{filter} is the reactive power of the filter for one inverter, Q is the quality factor, and N_{Inv} is the number of the parallel inverters. Q_{filter} is set from the inverter mask (see Section 2.2). The switching frequencies harmonics n1 and n2 are as follows

$$n_1 = \frac{f_{PWM}}{f_s} \quad (7)$$

$$n_2 = 2n_1 \quad (8)$$

where f_{PWM} is the PWM frequency and f_s is the nominal frequency.
In case another type of filter (LC or LCL filter) or other parameters should be used, the filter can be modified by the user inside the inverter subcircuit. If several inverters are found in the network, the filter subcircuit and its parents must be made unique to avoid modifying all inverters instances. Also, these filters can be excluded when REGC_A, REGC_C or AVM models are used.

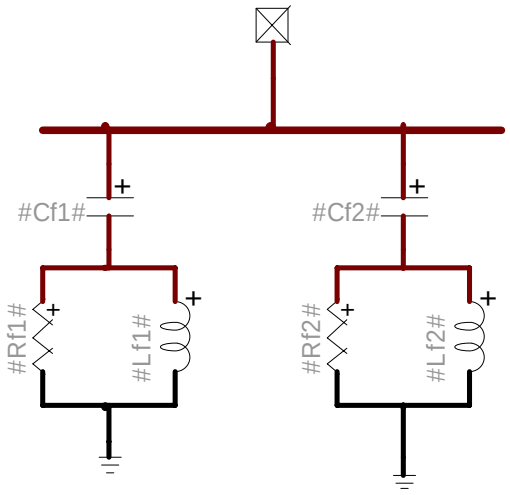


Figure 9 “shunt ac harmonic filter” block.

3.3 Converter control system

The EMTP diagram of the inverter control system block (or “Converter_control” block) is shown in Figure 10. The sampled signals are converted to pu and filtered by the data acquisition block. The sampling frequency are set to 12.5 kHz and can be modified by the user from the device mask. The “sampling” blocks are deactivated in AVM, REGC_A and REGC_C, due to large simulation

time step usage. In generic model, 2nd order Bessel type low pass filters (LPFs) are used. The cut-off frequencies of the filters are set to 2.5 kHz and can be modified by the user from the inverter device mask. The order (up to 8th order), the type (Bessel and Butterworth) and the cut-off frequencies of the low pass filters can be modified from device mask. The “LPF_GCS” blocks are deactivated in REGC_A and REGC_C. The protection block includes the AC over/under voltage protections, deep voltage sag detector, the DC chopper control, and overcurrent detector. The control system offers WECC REEC_D model for the outer loop control, and a generic model, WECC REGC_A model, or WECC REGC_C model options for the inner current loop control. User can select the control system options from the device mask (see Section 2.2). The data acquisition and control system models can run from a compiled code. Faster simulation time is obtained compared with the EMTP component-based model by using this option.

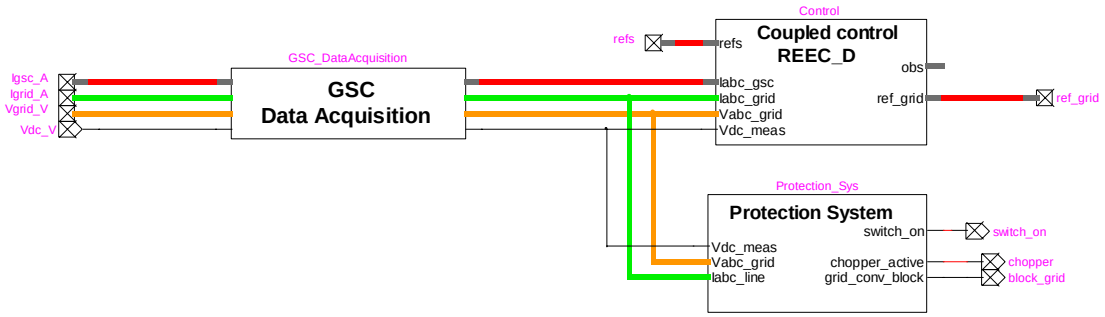


Figure 10 EMTP diagram of the PV inverter control block.

3.3.1 Computing variables block

The EMTP diagram of the “Computing Variables” and “Grid Control” block is shown in Figure 11. The “Computing Variables” block does the dq transformation required for the vector control. In “computing variable” block, a synchronous reference frame (SRF) PLL is used to drive the phase angle θ of the rotating reference frame from the inverter terminal voltages, allowing the synchronization of the control parameters with the system voltage [8], [9]. The EMTP diagram of the SRF PLL is shown in Figure 12. Moreover, two abc-to-dq frame transformations are used to transfer voltage and current sinusoidal waveforms to DC quantities (d and q reference frame) waveforms. The park transformation transforms abc-frame waveforms into dq-frame components rotating at synchronous speed $\omega = d\theta/dt$. In this transformation, the direct axis d is aligned with the grid voltage. If the PLL is in a steady-state condition, the q axis of the inverter voltage terminal is equal to zero [9]. The “Grid Control” block contains the outer and inner control loops.

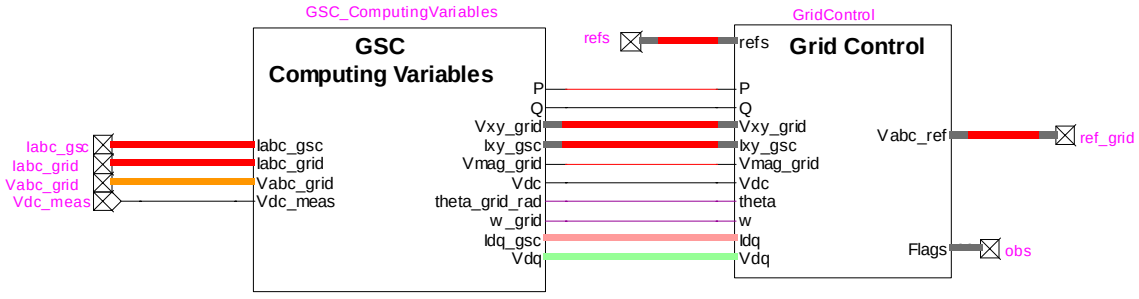


Figure 11 EMTP diagram of “coupled control + REEC_D” block.

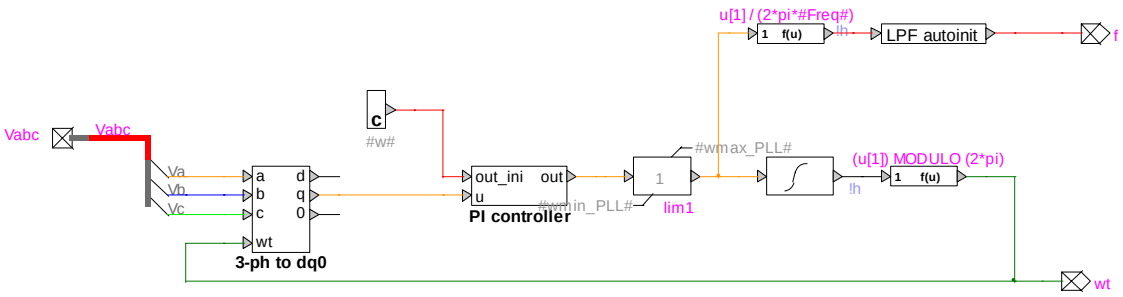


Figure 12 EMTP diagram of SRF PLL.

3.3.2 REEC_D model

REEC_D block is implemented according to [1] and [5] (see Figure 13). This block generates the inverter reference currents $Ipcmd$ and $Ipcmd$ (see Figure 14) from active power and reactive power references sent by power plant controller. This is the most recent inverter control model developed by WECC, which contains main new features, such as extended voltage-dependent current limit tables (VDLp, VLDq curves), local current compensation, local reactive -droop compensation, reactive-current injection algorithm, model inverter blocking logic. REEC_A or REEC_B can be converted to REEC_D with modifying some parameters. [5].

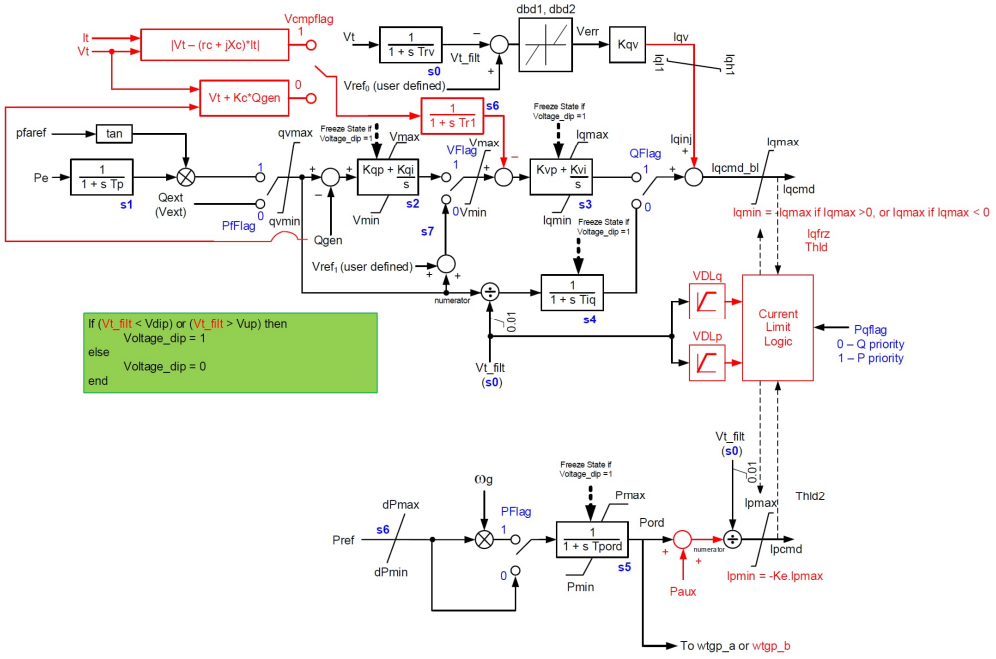


Figure 13 REEC_D model [1].

3.3.3 Generic current control

Figure 14 shows EMTP diagram of the “Grid Control” block. It is a current-controlled active and reactive controller in dq-frame. The active and reactive power of inverter are controlled by the line current components i_d $(or\ i_p)$ and i_q [4], [3],. The reference current commands i_{dref} and i_{qref} for the inner current loop are generated by outer loop control “REEC_D” and “Current ramp/limit control” blocks. In the inner current control and linearization blocks, the feedback and feed-forward signals in dq-frame are processed by compensators to make the control signals. Then, they are

transformed to the abc-frame and sent to the converter. The inner current loop design procedure is explained in detail in [3].

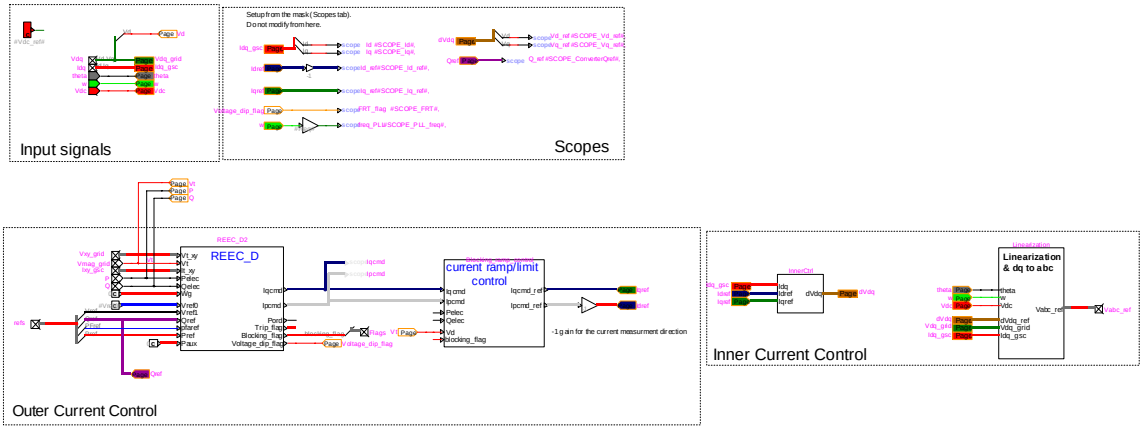


Figure 14 EMTP diagram of "control" block for REEC_D + generic current control model.

In "Current ramp/limit control" block, there are rate limiters to bound the command signals ($Ipcmd$ and $Ipcmd$) for recovery after fault, e.g., voltage rise or drop (see Section 2.2), before sending to the inner current loop. The implementation of this rate limiters is the same as the model used for the REGC_B model.

3.3.4 REGC_A model

Figure 15 shows EMTP diagram of the "REEC_D" and "REGC_A" blocks. Figure 16 shows the REGC_A model. As shown in Figure 16, the real active and reactive commands are passed through rate limiters and high voltage reactive current management and low voltage active current management blocks, and outputs real and reactive currents are injected to the grid by a simple current source (see Figure 7). The active and reactive current are transferred to abc frame at the synchronous reference frame angle calculated by a generic PLL as shown in Figure 17.

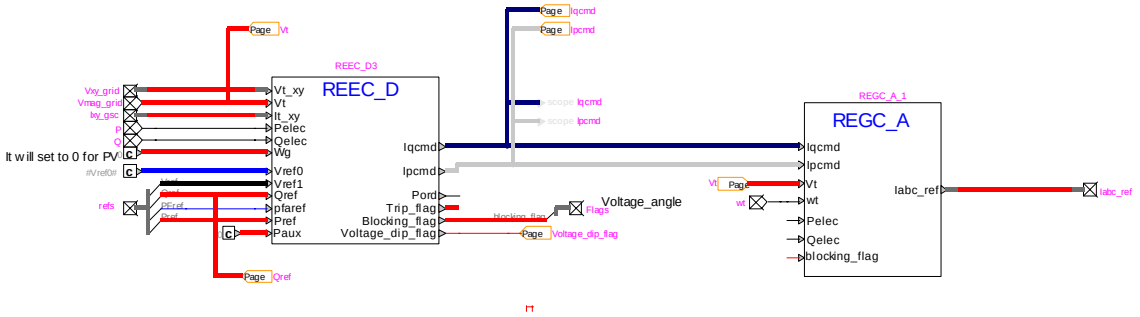


Figure 15 EMTP diagram of "control" block for REEC_D+REGC_A model.

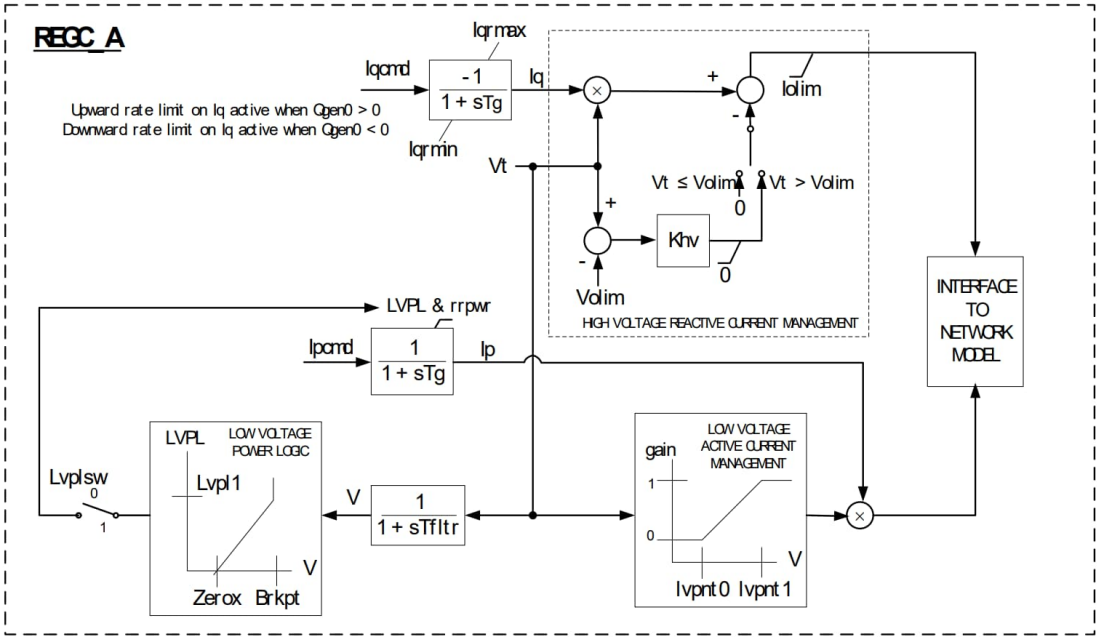


Figure 16 REGC_A model [2].

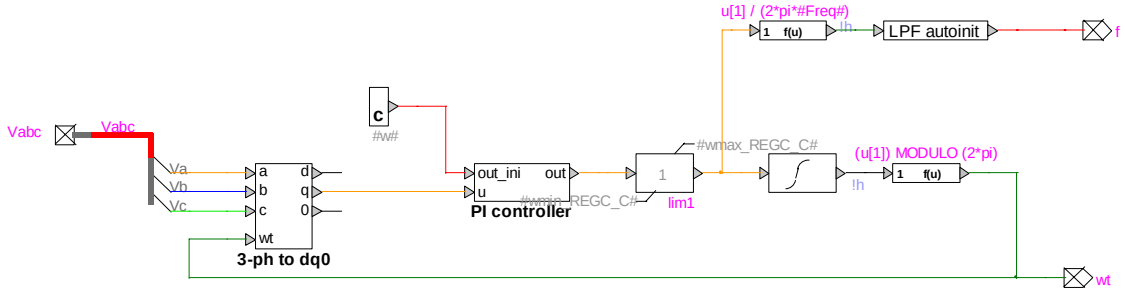


Figure 17 PLL model used in REGC_A + REEC_D model.

3.3.5 REGC_C model

Figure 18 shows EMTP diagram of the “REEC_D” and “RECG_C” block. Figure 19 shows the REGC_C model. A simplified representation of the inner-current loops and an algebraic equation that compute the required voltage at the inverter terminal to inject current into the network in response to active and reactive current commands from the REEC_D model.

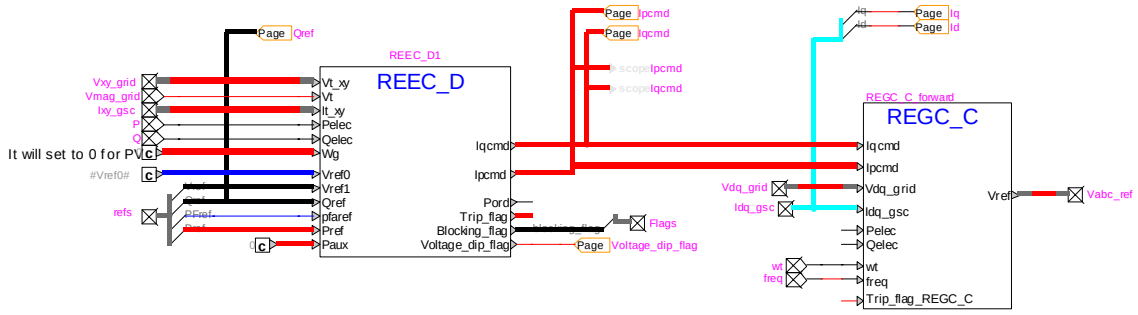


Figure 18 EMTP diagram of “control” block for REEC_D+REGC_C model.

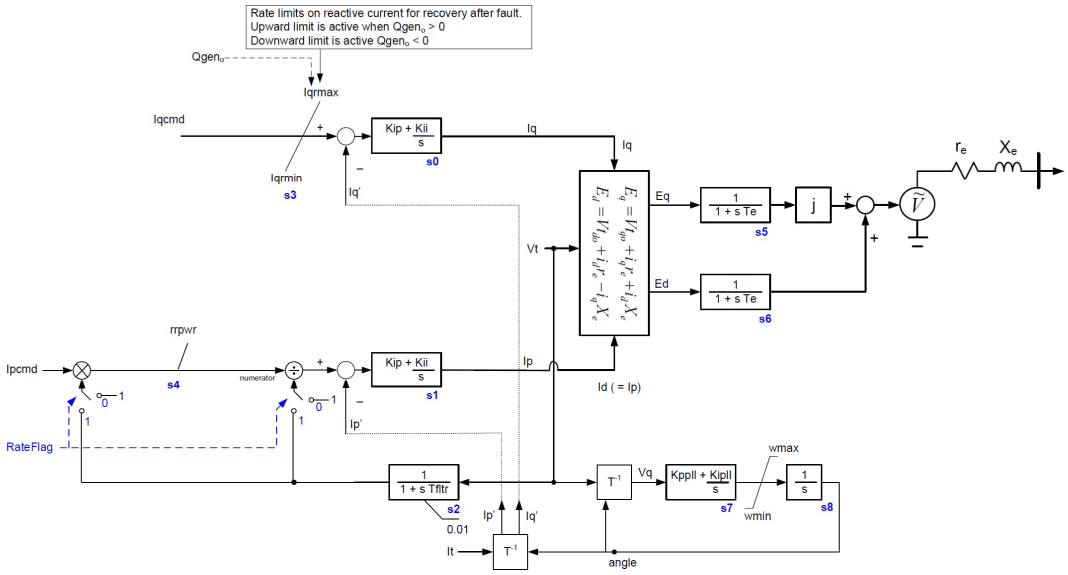


Figure 19 REGC_C model [1].

3.4 Inverter protection system block

The “protection system” block includes an over/under voltage relay, deep voltage sag detector, dc overvoltage protection and an overcurrent detector for each converter to protect IGBT devices when the system is subjected to overcurrent. For initialization, all protection systems, except for DC chopper protection, are activated after 300ms of simulation (i.e. init_Prot_delay = 0.3s). The protection system parameters (except over/under voltage relay) can be modified from the device mask (see Section 2.2).

3.4.1 Over/under voltage protections and deep voltage sag detector

The over/under voltage protections are designed based on the technical requirements set by Hydro Quebec for the integration of renewable generation. The over/under voltage limits as a function of time is presented in Figure 20 and can be modified in the inverter device mask. The voltages below the red line reference and above the black line reference correspond to the ride-through region where the inverter is supposed to remain connected to the grid.

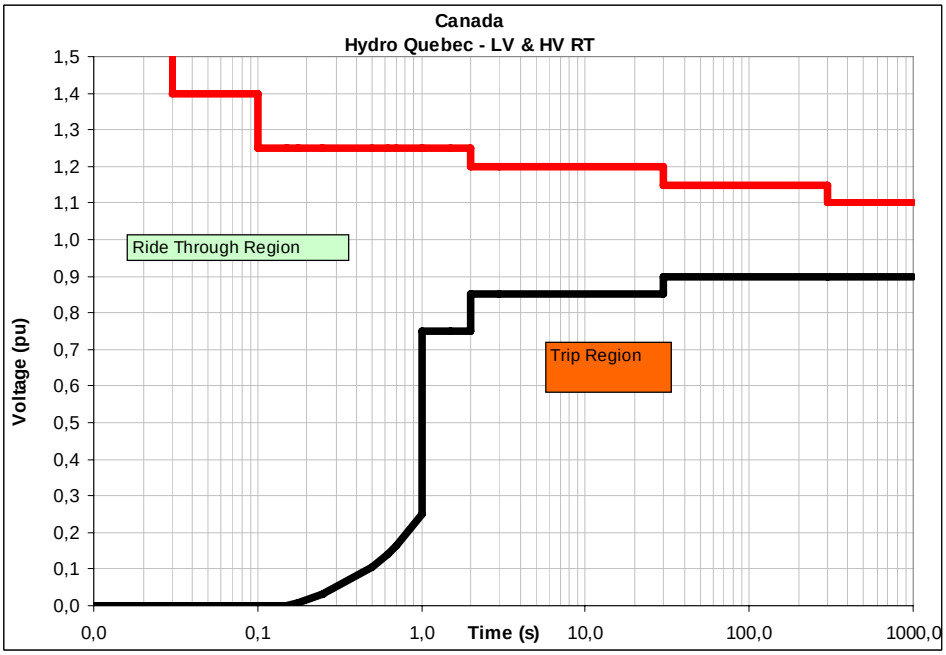


Figure 20 LVRT and HVRT requirements [10].

This block measures the rms voltages on each phase and sends a trip signal to the inverter circuit breaker when any of the phase rms voltage violates the limits in Figure 20 (see the upper part of Figure 22).

The instantaneous overvoltage protection suggested by IEEE Std 1547-2018 is developed and added to the protection schemes. This protection works based on cumulative instantaneous overvoltage. Figure 21 shows the threshold values of the voltage (per unit of nominal instantaneous peak base) and cumulative duration of the transient overvoltage protection, and they can be modified in the device mask. The cumulative duration is the sum of durations when the instantaneous voltage exceeds the protection threshold over a one-minute time window.

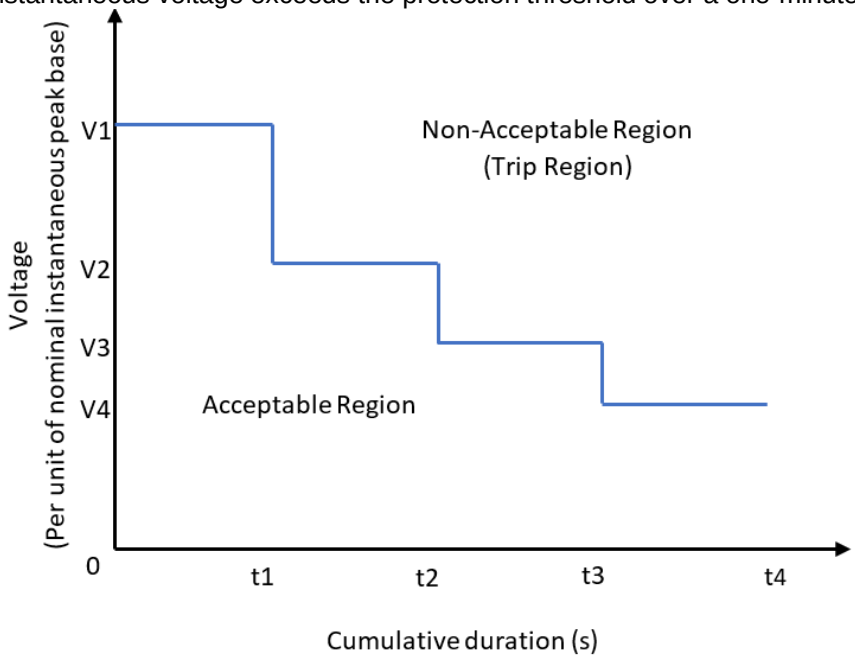


Figure 21 Transient overvoltage limits.

The “Deep Voltage Sag Detector” block (lower part of Figure 22) temporary blocks the Inverter in order to prevent potential overcurrent and restrict the FRT operation to the faults that occur outside the inverter.

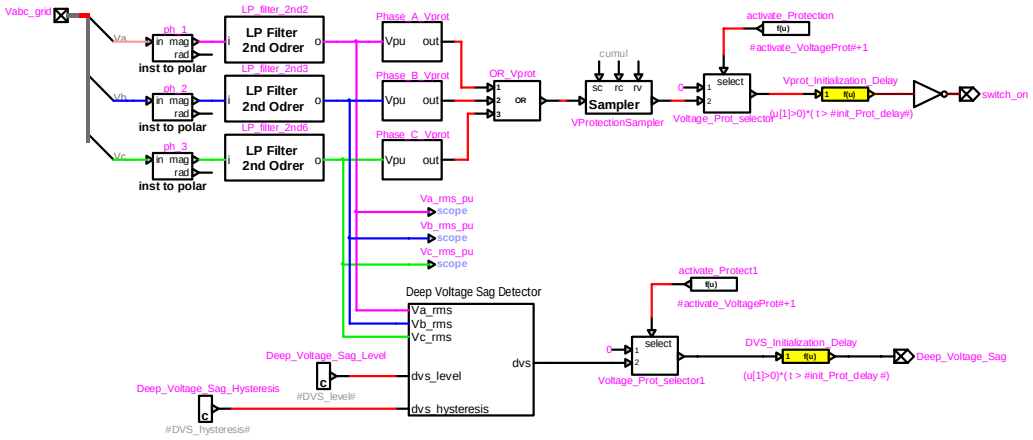


Figure 22 Over/under-voltage protections and deep voltage sag protections.

3.4.2 DC overvoltage protection block

The function of DC chopper is to limit the DC bus voltage. It is activated when the dc bus voltage exceeds $|U_{chopper-ON}|$ and deactivated when dc bus reduces below $|U_{chopper-OFF}|$. EMTP diagram of the “dc overvoltage protection” is shown in Figure 23. This protection is disabled for “REGC_A + REEC_D” and “REGC_C + REEC_D” converter models.

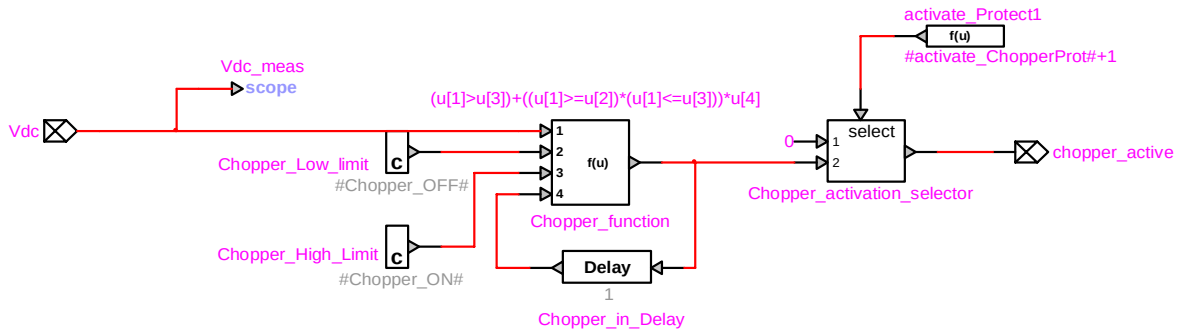


Figure 23 dc overvoltage protection block.

3.4.3 Overcurrent protection block

The overcurrent protection shown in Figure 24 blocks the converter temporarily when the converter current exceeds the pre-specified limit.

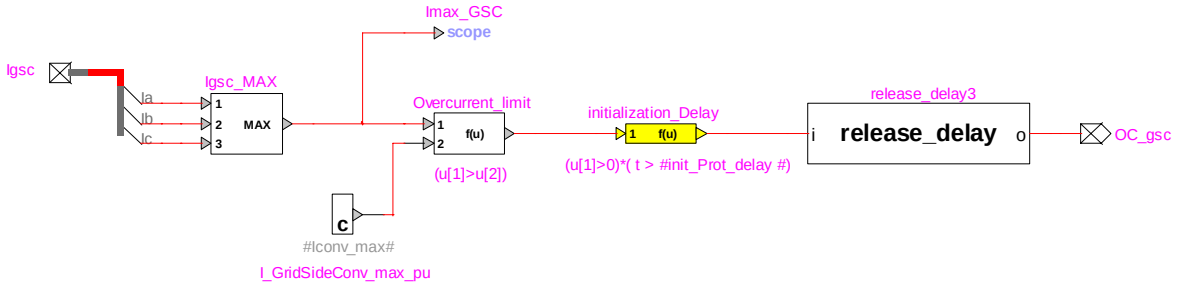


Figure 24 Overcurrent protection block.

3.5 Park controller

The function of park controller is to monitor the point of interconnection (POI) of a plant and sends real and reactive power/voltage/ power factor commands to inverters in the plant to control the real power and reactive power/voltage/power factor at the POI.
In EMTP (see PVPC block in Figure 1), REPC_A model is implemented according to model provided in [11] (see Figure 25).

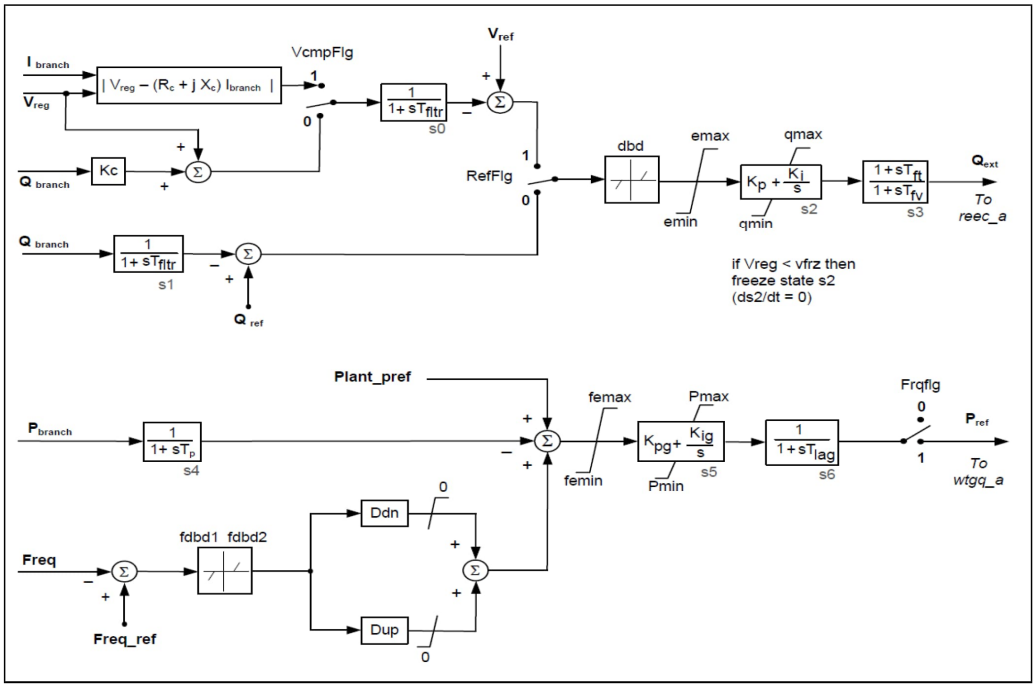


Figure 25 REPC_A model [11].

3.6 Inverter harmonic model

For harmonic analysis, the PV park is modeled with a harmonic Norton source. The harmonic study can be done in time domain, in which case **Use harmonic model for steady-state and time-domain simulations** must be checked or in the frequency domain with the frequency-scan simulation option, in which case **Use harmonic model for frequency-scan simulations**.
The harmonic currents are provided in percentage of the fundamental, for one inverter. The total park current is rescaled according to the number of inverters in service.
It is possible to automatically adjust the fundamental frequency current generated by each inverter and the harmonic current angles to match the load-flow results by checking Adjust fundamental frequency current to match Load-Flow results. When this box is checked, the I Angle input of the first line, which corresponds to the fundamental frequency current is adjusted to match the inverter current angle during the load-flow. The Fundamental frequency current magnitude is also adjusted to match the load-flow results. The fundamental frequency angle value is also added to the I Angle values of the other harmonics. Therefore, when this option is checked, the phase difference between the harmonic currents and the fundamental frequency current should be entered in the **I Angle** column.

4 PV Park Model Simulations

In this section, some simulation tests are performed to demonstrate some features of the Models. Figure 26 shows the network used for the simulation tests.

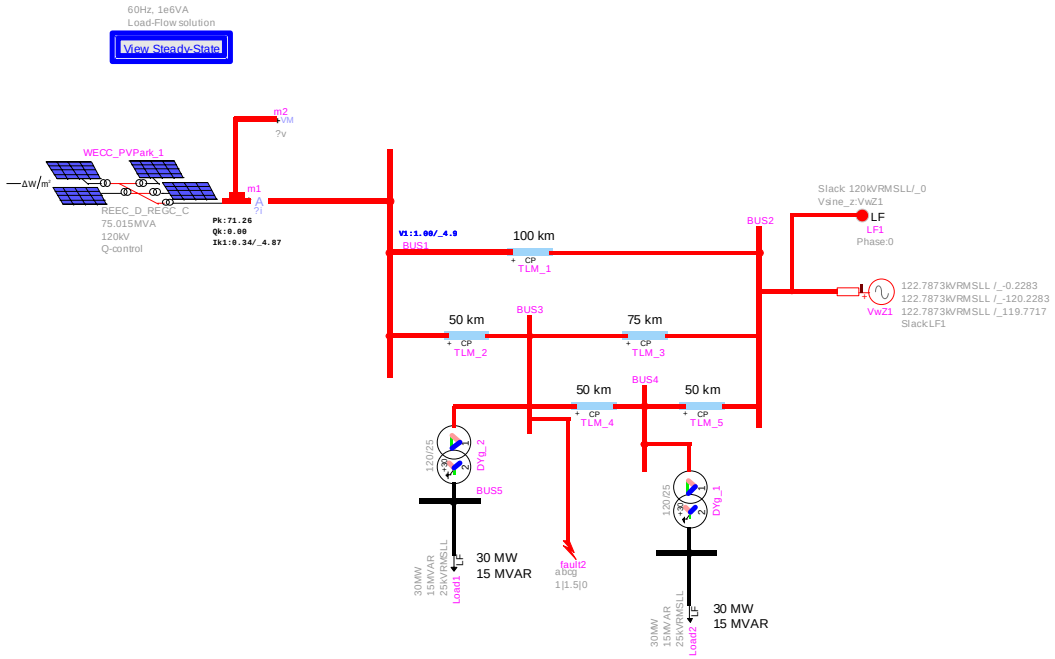


Figure 26 EPRI aggregated PV park network.

4.1 Active power and reactive control at POI

In this simulation, several active power and reactive power reference steps are applied to Pref and Qref inputs inside the “PVPC” block. Initially, the inverter generates 71.26MW (1pu) and 0MVAR. Figure 27 shows the active power and reactive power follow the reference changes. PI controller gains for the reactive and active power control are set to typical values.

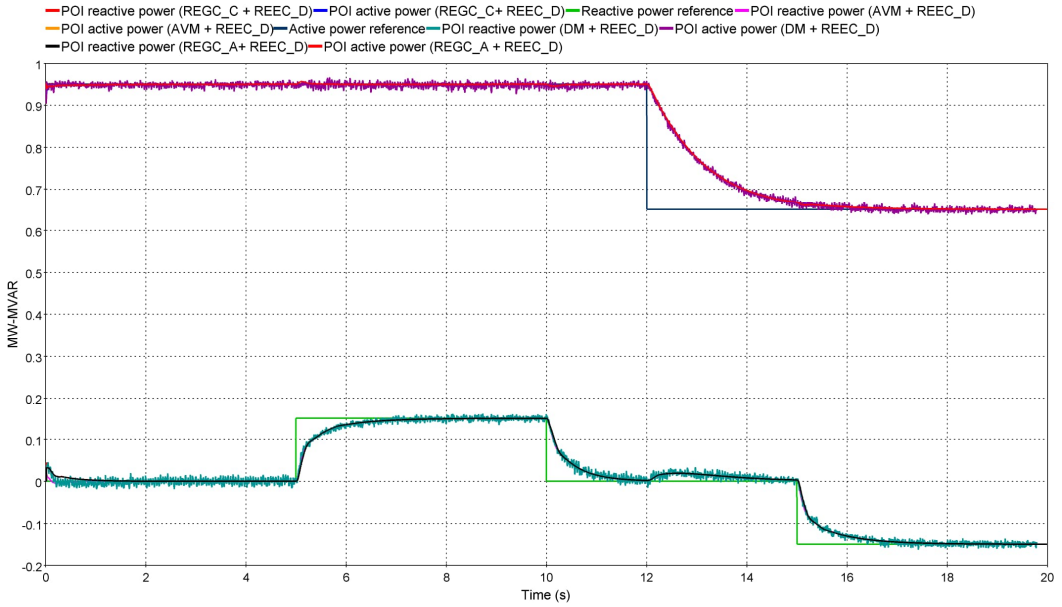


Figure 27 Active and reactive power control test.

4.2 Fault test

This test presents the model response during a fault. Fault duration is 0.5s, and the inverter initially generates 71.26MW and 0MVAR. During this event, the voltage drops to 0.22pu at POI.
Figure 28 shows the voltage at POI point, and Figure 29 shows inverter active and reactive power. The results for all converter types are presented.

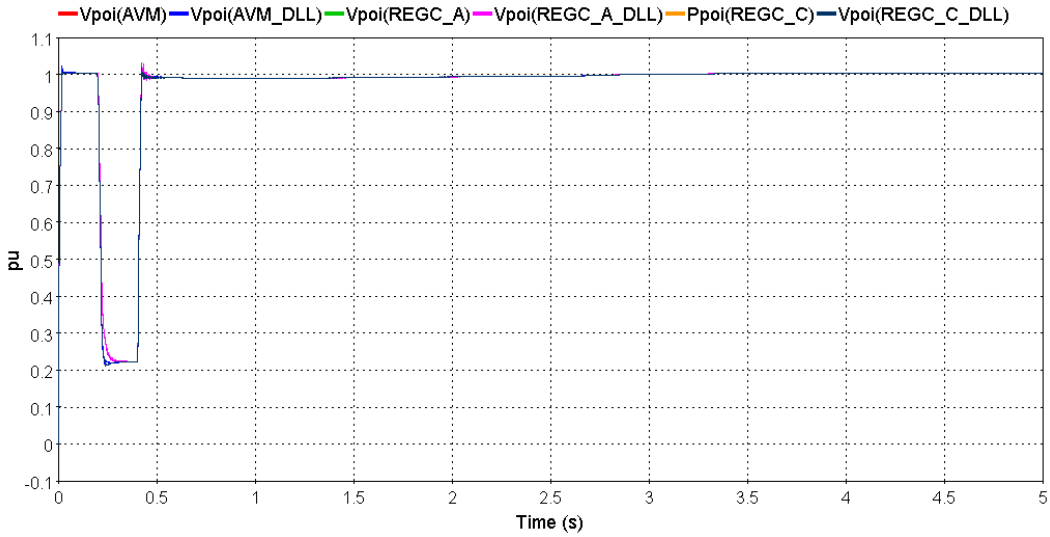


Figure 28 LVRT test: RMS voltage at POI.

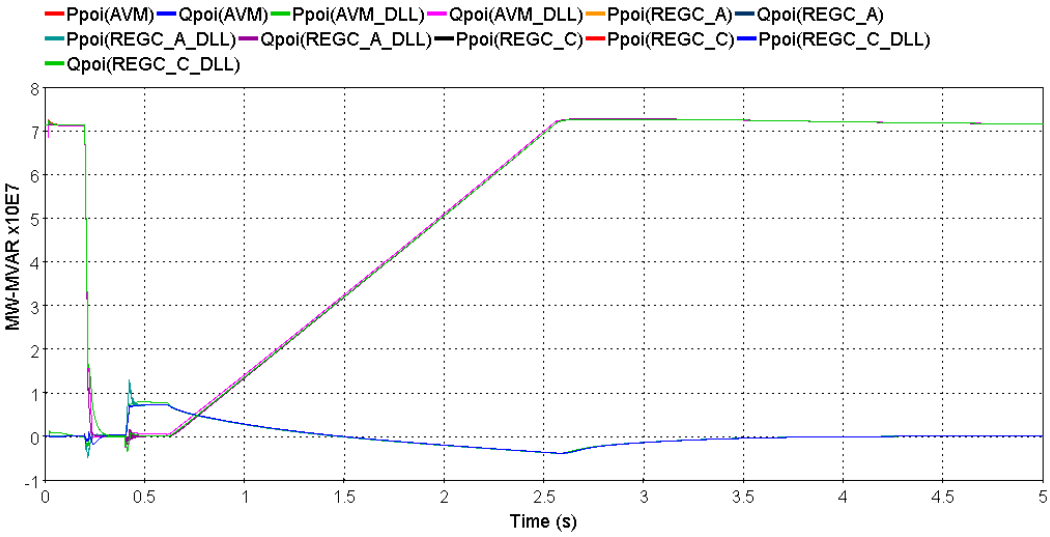


Figure 29 Fault test: POI active power, POI reactive power.

5 References

[1] "Proposal for new features for the renewable energy system generic models, Memo RES modeling updates Rev17," [Online]. Available: https://www.wecc.org/.

[2] "Proposed Changes to the WECC WT4 Generic Model for Type 4 Wind Turbine Generators," [Online]. Available: https://www.wecc.org/.

[3] U. Karaagac, J. Mahseredjian, R. Gagnon, H. Gras, H. Saad, L. Cai, I. Kocar, A. Haddadi, E. Farantatos, S. Bu, K. W. Chan and L. Wang, "A Generic EMT-Type Model for Wind Parks With Permanent Magnet Synchronous Generator Full Size Converter Wind Turbines," *IEEE Power and Energy Technology Systems Journal,* vol. 6, no. 3, pp. 131-141, Sept. 2019.

[4] A. Yazdani and R. Iravani, Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications, Wiley-IEEE Press, 2010.

[5] "Converting REEC_B to REEC_A/D for Solar PV Generators," [Online]. Available: https://www.wecc.org/.

[6] S. R. Sanders, J. M. Noworolski, X. Z. Liu and G. C. Verghese, "Generalized averaging method for power conversion circuits," in *ual IEEE Conference on Power Electronics Specialists*, San Antonio, TX, USA,, 1990.

[7] J. G. Slootweg, H. Polinder and W. L. Kling, "Representing wind turbine electrical generating systems in fundamental frequency simulations," *IEEE Transactions on Energy Conversion,* vol. 18, no. 4, pp. 516-524, 2003.

[8] G.-C. Hsieh and J. Hung, "Phase-locked loop techniques. A survey," *IEEE Transactions on Industrial Electronics,* vol. 43, no. 6, pp. 609-615, 1996.

[9] F. Blaabjerg, R. Teodorescu, M. Liserre and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics,* vol. 53, no. 5, pp. 1398-1409, 2006.

[10] "Transmission Provider Technical Requirements for the Connection of Power Plants to the Hydro-Quebec Transmission System," Hydro Quebec Transenergie, 2009.

[11] "WECC Wind Power Plant Dynamic Modeling Guid," [Online]. Available: https://www.wecc.org/.